Theory and Practical Implementation of Harmonic Resonant Rail Driver

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ABSTRACT

This paper presents a new algorithm for designing efficient harmonic resonant rail drivers. The circuit solution is coupled to a standard pulse source and uses only discrete passive components. It can thus be externally tuned to minimize the consumed power in the target IC. A new efficient algorithm based on current-fed pulse-forming network theory is proposed to find the value of each discrete component for a target frequency and a given load capacitance. The proposed driver topology can be used to generate any desired periodic 50% duty-cycle waveform by superimposing multiple harmonics of the desired waveform, however, this paper focuses on the generation of square-wave clock signals. We have tested the driver with a capacitive load between 38.3pF and 97.8pF. The overall dissipation for our second-order harmonic rail driver is 19% of fCV^2 at 15MHz and 97.8pF load.

Keywords

Harmonic-resonant rail driver, energy-recovery circuit, pulse-forming network, clock generation.

1. INTRODUCTION

The clocking circuitry of a VLSI chip is a significant source of power dissipation in many cases [1]. Reducing the power dissipated inside the clock drivers and clock signal lines can significantly reduce the overall power dissipation of the VLSI system. Since for CMOS VLSI the clock signal line loads are highly capacitive, it is possible to use resonant charging techniques to dissipate only a small fraction of the energy stored in the clock lines during each clock cycle. The simplest approach is to use a flyback circuit shown in Fig. 1 that will produce sinusoidal pulse [2]. In spite of its simple structure, energy efficiency of the driver is relatively poor when the nFET is driven non-resonantly. Blip circuits (Fig. 2) [3] have been successfully demonstrated that all-resonant almost non-overlapping sinusoidal pulses can be generated by cross-coupling two such circuits. These pulses have been used as a source of cheap power for driving the large on-chip CMOS signal lines of a VLSI microprocessor [2][4] and can also be used as a two-phase clock.

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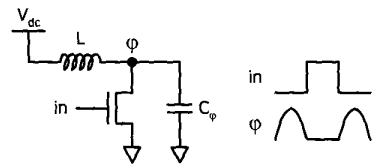

Fig. 1: A single-rail resonant clock driver

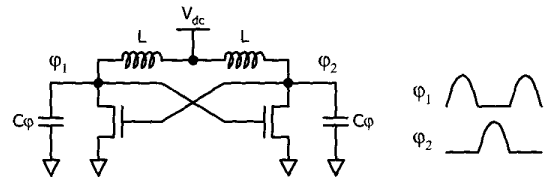

Fig. 2: The all-resonant blip driver

A common disadvantage of both these drivers is that the output signal frequency and magnitude depend heavily on the load capacitances $C\varphi$. Because the load capacitances $C\varphi$ may be data-dependent and can vary from cycle to cycle, these clock drivers can exhibit some frequency variation, which adversely affects system stability and performance [5]. Of the two drivers, frequency variation in the blip driver is often more pronounced because of the positive-feedback nature of the two outputs. Another disadvantage of both of these drivers is the need for a distinct power supply V_{dc} whose value is determined by the load capacitance and the target frequency.

The slow rise and fall times of the sinusoidal pulse is another major concern for non-adiabatic applications for two reasons. First, the slow transition times generally increase the amount of short circuit current in internal clock drivers and/or clock-related circuits, i.e., flip-flops and latches. To overcome this problem, designers are forced to use lower than nominal supply voltages to limit short circuit current, thereby reducing achievable performance. Second, the speed penalty imposed by the slow transition times of sinusoidal pulses can be a significant portion of the cycle time, making them often impractical. A resonant rail driver with faster transition times can overcome these difficulties, making it applicable to both adiabatic and non-adiabatic applications.

Younis and Knight [6] proposed a non-dissipative rail driver to generate square-wave signals resonantly. However, depending on the number of harmonically related sinusoids in the output signal, their circuit requires several distinct power supplies, which are prohibitive for practical implementations.

In this paper, we present a new algorithm and experimental results for harmonic resonant rail driver circuits that generate desired

waveforms with 50% duty cycle by superimposing multiple harmonics. Linear network theory is normally applied to predict the waveform that would be generated by a network of passive components. We seek to apply it for the inverse problem, i.e., given a waveform, derive the network of passive components. An incremental solution to this problem was proposed in [6]. In our work, however, we have developed a direct method for calculating the component values given the desired waveform shape and the nominal value of the load capacitance. We have experimentally validated the theory for generating waveforms approximating square waves. Our algorithm is based on current-fed pulse-forming network theory [7]. Traditionally, these current-fed networks are powered by a constant current source, which can often consume significant power. In contrast, we propose using a conventional pulse generator so that no additional distinct voltage or current supply is needed.

Our circuit topology has been tested for various load capacitances at frequencies up to 15MHz. The worst-case overall dissipation for a second-order harmonic signal is 19% of fCV^2 at 15MHz and 97.8pF load. Frequency variation due to a change in load capacitance is minimal because the input pulse generator serves as a continuous correcting factor. In addition, the stable input pulse level substantially suppresses variation of the peak voltage. Variations in the load capacitance appear as higher dissipation in the clock driver.

The remainder of this paper is organized as follows. First, we briefly review the theory of waveform synthesis using a current-fed pulse-forming network. Then, we present our new algorithm to identify the value of each component in the proposed driver. We then discuss practical implementations and laboratory measurement results. We conclude by discussing potential applications and future work.

2. CURRENT-FED PULSE-FORMING NETWORKS

One way to generate an arbitrary periodic pulse is to exploit its Fourier series expansion by superimposing a finite number of its harmonics. In particular, an ideal square-wave $v(t)$ can be represented using the following infinite series.

$$v(t) = \frac{2V_0}{\pi}\sin\frac{2\pi t}{T} + \frac{2V_0}{3\pi}\sin\frac{6\pi t}{T} + \frac{2V_0}{5\pi}\sin\frac{10\pi t}{T} + \cdots \qquad (1)$$

where T is the period of the square-wave. In practice, only the first few terms are needed to yield a waveform that closely approximates a square-wave.

A current-fed pulse-forming network (CFPN) yielding the first n harmonics is shown in Fig. 3 [7]. To analyze this network, we first assume that switch S opens at $t=0$ and there is no energy initially stored in the network.

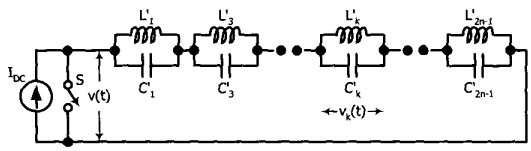

Fig. 3: Current-fed pulse-forming network (CFPN)

The voltage across k-th LC-section is shown in Eq. 2.

$$v_k(t) = I_{DC}\sqrt{\frac{L_k'}{C_k'}}\sin\frac{t}{\sqrt{L_k'C_k'}} \qquad (2)$$

Cascading n such a LC-section in series yields the following equation for the output voltage $v(t)$.

$$v(t) = \sum_{k=1,3,\ldots}^{2n-1} I_{DC}\sqrt{\frac{L_k'}{C_k'}}\sin\frac{t}{\sqrt{L_k'C_k'}} \qquad (3)$$

By comparing Eq. 3 with Eq. 1, the values of all components in the network can be directly determined.

As is, however, this network cannot directly be used as a driver because none of the capacitances model the load capacitance residing between the output node and ground. To meet this requirement, an equivalent network can be derived through mathematical transformations of impedance and admittance functions as shown in the following equations.

$$Z(s) = \sum_{k=1,3,\ldots}^{2n-1} \frac{L_k's}{L_k'C_k's^2+1} \qquad (4)$$

$$Y(s) = \frac{1}{Z(s)} = \frac{\prod_{k=1,3,\ldots}^{2n-1}(L_k'C_k's^2+1)}{\sum_{k=1,3,\ldots}^{2n-1} L_k's\prod_{\substack{i=1,3,\ldots\\ i\neq k}}^{2n-1}(L_i'C_i's^2+1)} = \frac{A_0}{s} + A_n s + \sum_{k=1}^{n-1}\frac{A_k}{B_k s^2+1} \qquad (5)$$

Fig. 4 depicts one of the equivalent networks of Fig. 3 that corresponds to Eq. 5. By inspection,

$$C_0 = A_n,\ L_0 = \frac{1}{A_0},\ L_k = \frac{B_k}{A_k},\ C_k = A_k \qquad (6)$$

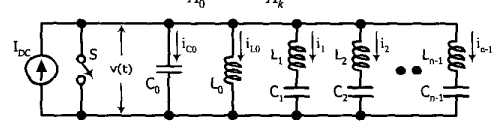

Fig. 4: Equivalent network of Fig. 3 where C_0 represents the on-chip capacitance load

The values for C_0 and L_0 are found by noting that

$$L_0 = \lim_{s\to 0}\frac{Z(s)}{s} = \sum_{k=1,3,\ldots}^{2n-1} L_k'$$
$$\frac{1}{C_0} = \lim_{s\to\infty} sZ(s) = \sum_{k=1,3,\ldots}^{2n-1}\frac{1}{C_k'} \qquad (7)$$

To find values of other components, we can use partial fraction expansion of the admittance function $Y(s)$ [8]. In the following section, we show that this incremental procedure can be replaced by finding the roots of a characteristic equation and solving a corresponding set of linear equations.

3. ALGORITHM

Since the two networks shown in Fig. 3 and Fig. 4 are equivalent, we can write the Laplace transform of $v(t)$ by converting Eq. 1 for the order of n, i.e.,

$$V(s) = \frac{2V_0\omega_0}{\pi}\left(\frac{1}{s^2+\omega_0^2} + \cdots + \frac{1}{s^2+(2n-1)^2\omega_0^2}\right) \qquad (8)$$

It is straightforward to get the Laplace transform for each branch current using Eq. 8 as follows.

$$I_{C0}(s) = \frac{2V_0C_0\omega_0}{\pi}\left(\frac{s}{s^2+\omega_0^2}+\cdots+\frac{s}{s^2+(2n-1)^2\omega_0^2}\right) \tag{9}$$

$$I_{L0}(s) = \frac{2V_0\omega_0}{\pi L_0}\left(\frac{1}{s(s^2+\omega_0^2)}+\cdots+\frac{1}{s(s^2+(2n-1)^2\omega_0^2)}\right) \tag{10}$$

$$\begin{aligned} I_k(s) &= \frac{1}{L_k}\frac{s}{s^2+\frac{1}{L_kC_k}}V(s) \\ &= \frac{2V_0\omega_0}{\pi L_k}\frac{1}{s^2+\omega_k^2}\left(\frac{s}{s^2+\omega_0^2}+\cdots+\frac{s}{s^2+(2n-1)^2\omega_0^2}\right) \\ &= \frac{2V_0\omega_0}{\pi L_k}\left(\frac{A_{k1}s}{s^2+\omega_k^2}+\frac{B_{k1}s}{s^2+\omega_0^2}+\cdots+\frac{A_{kn}s}{s^2+\omega_k^2}+\frac{B_{kn}s}{s^2+(2n-1)^2\omega_0^2}\right) \end{aligned} \tag{11}$$

where

$$\left.\begin{aligned} &\omega_k = 1/\sqrt{L_kC_k}, \\ &A_{kj}+B_{kj}=0 \\ &A_{kj}(2j-1)^2\omega_0^2+B_{kj}\omega_k^2=1 \\ &\sum_{j=1}^{n}A_{kj}=0 \end{aligned}\right\} \text{for } 1\le j\le n \tag{12}$$

The last condition in Eq. 12 should be satisfied to prevent the L_kC_k-section from introducing a new pole at ω_k. The second and third conditions can be derived from a partial fraction expansion of the Eq. 11. These conditions are combined to produce a characteristic equation,

$$\begin{aligned} A_{kj}((2j-1)^2\omega_0^2-\omega_k^2)&=1 \\ A_{kj}&=\frac{1}{(2j-1)^2\omega_0^2-\omega_k^2} \\ \therefore \sum_{j=1}^{n}A_{kj} &= \frac{1}{\omega_0^2}\sum_{j=1}^{n}\frac{1}{(2j-1)^2-x}=0, \text{ where } x=\left(\frac{\omega_k}{\omega_0}\right)^2 \end{aligned} \tag{13}$$

Let's assume that n-1 roots of this characteristic equation are found, that is,

$$\omega_1^2=\alpha_1\omega_0^2, \omega_2^2=\alpha_2\omega_0^2, \ldots, \omega_{n-1}^2=\alpha_{n-1}\omega_0^2 \tag{14}$$

By applying KCL on the output node of the network, the relationship of branch currents is defined by the equation

$$\begin{aligned} &\frac{I_{DC}}{s}-I_{C0}(s)=I_{L0}(s)+\sum_{k=1}^{n-1}I_k(s) \\ &\frac{I_{DC}}{s}-\frac{2C_0V_0\omega_0}{\pi}\left(\frac{s}{s^2+\omega_0^2}+\cdots+\frac{s}{s^2+(2n-1)^2\omega_0^2}\right) \\ &=\frac{2V_0}{\pi L_0\omega_0}\left(1+\frac{1}{3^2}+\cdots+\frac{1}{(2n-1)^2}\right)\frac{1}{s} \\ &-\frac{2V_0}{\pi\omega_0}\left(\frac{1}{L_0}+\frac{1}{L_1(1-\alpha_1)}+\cdots+\frac{1}{L_{n-1}(1-\alpha_{n-1})}\right)\frac{s}{s^2+\omega_0^2} \\ &-\frac{2V_0}{\pi\omega_0}\left(\frac{1}{3^2L_0}+\frac{1}{L_1(3^2-\alpha_1)}+\cdots+\frac{1}{L_{n-1}(3^2-\alpha_{n-1})}\right)\frac{s}{s^2+3^2\omega_0^2} \\ &-\cdots \\ &-\frac{2V_0}{\pi\omega_0}\left(\frac{1}{(2n-1)^2L_0}+\cdots+\frac{1}{L_{n-1}((2n-1)^2-\alpha_{n-1})}\right)\frac{s}{s^2+(2n-1)^2\omega_0^2} \end{aligned} \tag{15}$$

Comparing both sides of Eq. 15, the linear equations shown in Eq. 16 determine the inductance values $L_1,\ldots,L_{n-1}$. These values are combined with Eq. 14 to calculate the capacitance values $C_1,\ldots,C_{n-1}$.

$$\begin{bmatrix} 1 & \frac{1}{1-\alpha_1} & \cdots & \frac{1}{1-\alpha_{n-1}} \\ \frac{1}{3^2} & \frac{1}{3^2-\alpha_1} & \cdots & \frac{1}{3^2-\alpha_{n-1}} \\ \cdots & \cdots & \cdots & \cdots \\ \frac{1}{(2n-1)^2} & \frac{1}{(2n-1)^2-\alpha_1} & \cdots & \frac{1}{(2n-1)^2-\alpha_{n-1}} \end{bmatrix}\begin{bmatrix} \frac{1}{L_0} \\ \frac{1}{L_1} \\ \cdots \\ \frac{1}{L_{n-1}} \end{bmatrix}=\begin{bmatrix} C_0\omega_0^2 \\ C_0\omega_0^2 \\ \cdots \\ C_0\omega_0^2 \end{bmatrix} \tag{16}$$

As an example, consider the task of finding the value of all components of the second-order driver for a 1MHz clock and a 100pF load. From Eq. 13, we have

$$\begin{aligned} &\frac{1}{1-x}+\frac{1}{9-x}=0 \\ &\therefore x=\alpha_1=5 \end{aligned} \tag{17}$$

Using this value, we can rewrite Eq. 16 as follows.

$$\begin{bmatrix} 1 & \frac{1}{1-5} \\ \frac{1}{3^2} & \frac{1}{3^2-5} \end{bmatrix}\begin{bmatrix} \frac{1}{L_0} \\ \frac{1}{L_1} \end{bmatrix}=100\times10^{-12}\left(\frac{2\pi}{10^{-6}}\right)^2\begin{bmatrix} 1 \\ 1 \end{bmatrix} \tag{18}$$

By solving these equations, we find inductor values, L_0=140.72uH and L_1=79.16uH. Lastly, since $\omega_1^2=5\omega_0^2=1/L_1C_1$, it follows that C_1=64pF.

4. IMPLEMENTATION

Even though the CFPN shown in Fig. 4 has an appropriate configuration for our applications, two problems preclude the network from being directly applied as a clock driver. First, the waveform swings between $+V_0$ and $-V_0$ as opposed to 0 to $+V_0$ swing. Second, the need for a constant current source is a major disadvantage of the CFPN. In particular, the benefit of low-power consumption of the CFPN would be cancelled out in the presence of a constant current source that generally consumes large amounts of power. We propose a unique solution that overcomes these impediments.

A voltage pulse-fed positive-swing pulse driver circuit is shown in Fig. 5. To generate the first n harmonic sinusoids at the output, we must filter out most of the sinusoids of higher frequencies present in the input square-wave pulse. This can be done by placing a resistance R between the input pulse generator and the output of the driver. Since the driver circuit is designed to resonate at the first n-th harmonic frequencies, ideally these sinusoids will not be affected by the resistance.

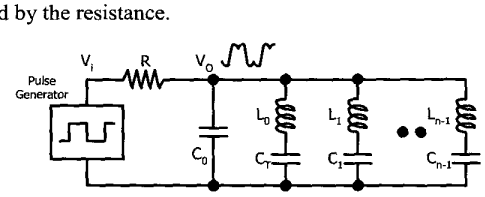

Fig. 5: Voltage pulse-fed harmonic resonant rail driver

Fig. 6 depicts the frequency response of the second-order driver circuit for a 1MHz clock signal with different resistance values. It is clearly shown that no distortion is incurred at two resonant frequencies (1MHz and 3MHz) for all resistance values. From this graph, it seems favorable to increase the resistance to reject higher harmonics. However, parasitic resistances of the components and

wires reduce the voltage level of output signal as R becomes larger. Therefore, it is important to use an adequate resistance value while maintaining proper voltage levels of the output signal for low-power dissipation. For driving 97.8pF load capacitance at 1MHz, test measurement demonstrates that 15% of fCV^2 was dissipated with 2kΩ resistance.

To make the output signal to swing positively, a large capacitance C_T is connected in series with L_0. In particular, due to its small impedance the required DC voltage across C_T ($1/2V_H$ of the input clock signal) can be successfully induced without affecting the resonant characteristic of the driver. In our lab tests, 100nF off-the-shelf capacitor was enough to achieve the desired DC voltage.

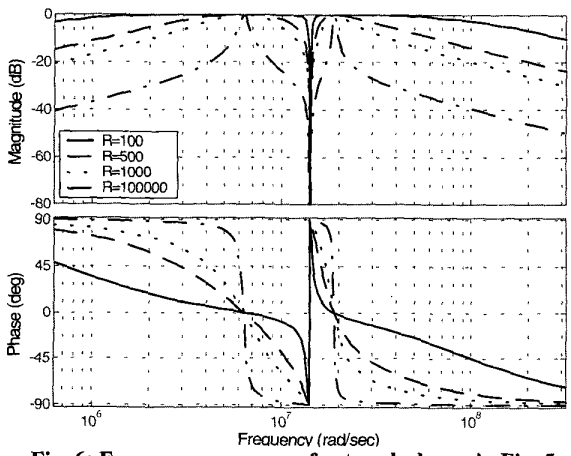

Fig. 6: Frequency response of network shown in Fig. 5 ($V_o(s)/V_i(s)$)

5. MEASUREMENTS

The harmonic resonant rail drivers containing up to four terms (i.e., fourth order) were designed and tested on a wire-wrap board that included tunable inductors and capacitors. We varied the frequency from 0.8 to 15MHz by setting these components to theoretical values we calculated using Eq. 16. We then tuned each component to achieve minimum measured power dissipation and compared them with their theoretical value. Testing at higher frequency was limited by the test setup and equipment that are available to the authors.

Table 1 summarizes the lab measurement results for various configurations. In most cases, the measured values of the components are within 7% of the theoretical values. Deviation between the theoretical and tuned capacitance values is larger than for the inductors presumably because of the large parasitic capacitances in our wire-wrapped board. As reported in Table 1, approximately 19% of the calculated conventional power dissipation fCV^2 was dissipated for the second-order driver at 15MHz to drive 97.8pF load capacitance. Power dissipation increases as the order of the driver increases. This effect appears to be due to more parasitic components in the test board. In addition, tuning the circuit for minimum measured power dissipation is increasingly error prone since more design variables are involved.

The last row in Table 1 shows the measurement data of the second order driver for different load capacitances at 1MHz. Resistance values are reduced to achieve 10% rising and falling times of the total cycle time. Power dissipation is increased by approximately 7% for this case while rising and falling times are shortened by 3% from the minimal power dissipation mode. This result suggests that by changing resistance value, we can control the rising and falling times at the expense of power consumption. Fig. 7 illustrates the measured power dissipation as we changed the resistance value R for 1MHz and 100pF. The transition time with 2kΩ resistance was measured as 110ns and other transition times are normalized in the graph. At 285Ω, the transition time drops to 50ns (45%) while the power dissipation increases from 15% to 57.9% of fCV^2.

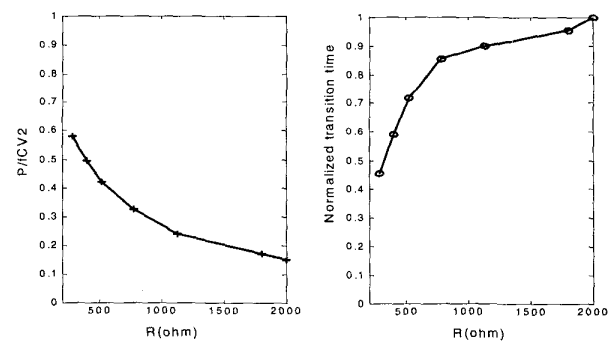

Fig. 7: Normalized power dissipation and transition time versus resistance R. fCV^2 is the theoretical conventional power dissipation to drive load capacitance C

Fig. 8 and Fig. 9 show oscilloscope traces of the output signal of the driver for the second and third order harmonics. To see how the output signal is synchronized, the input pulse is also shown. FFT-enabled oscilloscope trace for the fourth-order driver output is presented in Fig. 10. It is shown in the figure that only four harmonic frequencies are present in the output signal. Fig. 11 presents the trace of the output signal of the second order harmonic driver for 10MHz frequency.

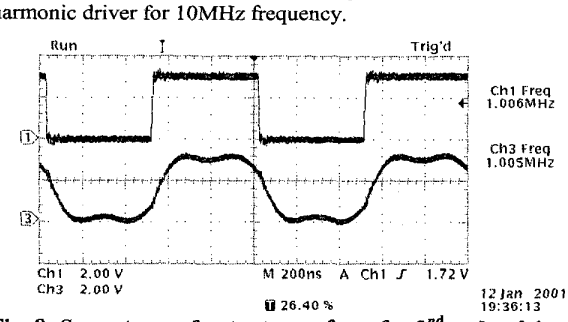

Fig. 8: Scope trace of output waveform for 2nd-order driver at 1MHz

To measure power dissipation and frequency variation as a function of load capacitance change, we varied the load capacitance C_0 from −30% to +30% of the nominal value while keeping all other components the same. The power was then measured. The results for a 1MHz clock and a 100pF load capacitance are plotted in Fig. 12. Normalized power dissipation in the graph is the ratio between the measured power dissipation and fCV^2. Power dissipation at 100pF is minimum because the

Table 1: Measured data of second, third and fourth harmonic resonant rail driver for various clock frequencies and load capacitances. The first three rows are data for driving 97.8pF load capacitance at different clock frequencies and the last row shows data for different load capacitances at 1MHz. Theoretical and measured values of each component are also shown for comparison.

	f_{CLK}	C0	C1		C2		C3		L0		L1		L2		L3		R	P/fCV^2
	MHz		theory	measured	theory	measured	theory	measured	Theory	measured	theory	measured	theory	measured	theory	measured		(%)
2nd order V_H=3 V_L=0	0.8	97.8	62.6	59.8	-	-	-	-	224.83	215.0	126.47	119.6	-	-	-	-	3.151	14.29
	1.0	97.8	62.6	59.8	-	-	-	-	143.89	135.9	80.94	75.6	-	-	-	-	2.015	14.53
	2.0	97.8	62.6	59.0	-	-	-	-	35.97	34.6	20.23	18.8	-	-	-	-	1.183	14.88
	5.0	97.8	62.6	59.3	-	-	-	-	5.76	5.6	3.24	2.96	-	-	-	-	0.493	14.66
	10.0	97.8	62.6	56.0	-	-	-	-	1.44	1.50	0.81	0.79	-	-	-	-	0.120	16.58
	15.0	97.8	62.6	56.5	-	-	-	-	0.64	0.67	0.36	0.36	-	-	-	-	0.056	19.00
3rd order V_H=3 V_L=0	0.8	97.8	105.3	98.8	21.4		-	-	155.28	155.2	81.49	80.3	98.84	94.8	-	-	2.311	16.45
	1.0	97.8	105.3	99.5	21.4	19.5	-	-	99.38	99.7	52.15	50.7	63.26	61.8	-	-	1.671	16.61
	2.0	97.8	105.3	100.1	21.4	19.4	-	-	24.84	24.3	13.04	12.6	15.81	15.3	-	-	0.879	16.78
	5.0	97.8	105.3	103.5	21.4	19.3	-	-	3.98	3.9	2.09	1.9	2.53	2.3	-	-	0.353	17.48
4th order V_H=3 V_L=0	0.8	97.8	146.4	137.0	33.2	30.8	11.7	10.2	118.53	117.5	60.86	60.8	66.68	67.0	83.15	78.0	1.417	26.41
	1.0	97.8	146.4	138.3	33.2	30.4	11.7	9.9	75.86	76.6	38.95	39.8	42.68	43.8	53.22	50.0	0.958	28.03
	2.0	97.8	146.4	138.0	33.2	31.4	11.7	9.9	18.96	19.2	9.74	9.7	10.67	10.7	13.30	12.0	0.617	27.16
	5.0	97.8	146.4	138.2	33.2	31.8	11.7	10.3	3.03	2.9	1.56	1.5	1.71	1.6	2.13	2.1	0.223	28.52
2nd order V_H=3 V_L=0	1.0	38.2	24.4	21.6	-	-	-	-	368.39	350.0	207.32	199.6	-	-	-	-	2.48	23.85
	1.0	55.4	35.5	34.2	-	-	-	-	254.01	243.3	142.88	138.4	-	-	-	-	1.867	23.27
	1.0	67.7	43.3	45.5	-	-	-	-	207.86	198.0	116.92	109.3	-	-	-	-	1.592	22.73
	1.0	84.0	53.8	56.0	-	-	-	-	167.53	160.30	94.23	90.10	-	-	-	-	1.577	22.76

circuit is designed to harmonically resonate at this value. Virtually no frequency variation was noticed for this range of capacitances. This is in sharp contrast to previously reported rail drivers whose frequency varies proportional to the square root of variations in capacitance [5]. For capacitance greater than 130%, however, slow transition times and low voltage swings are observed. On the other hand, if we reduce the load capacitance below 70% of nominal, the power dissipation increases rapidly because current from the input pulse generator charges the load capacitance instead of it being charged resonantly.

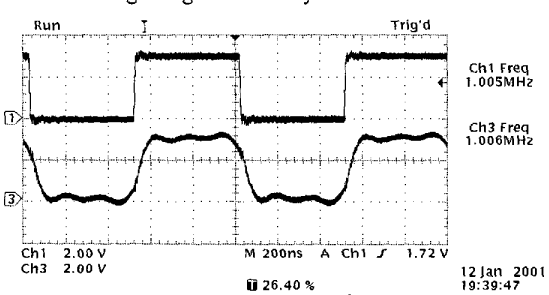

Fig. 9: Scope trace of waveform for 3rd-order driver at 1MHz

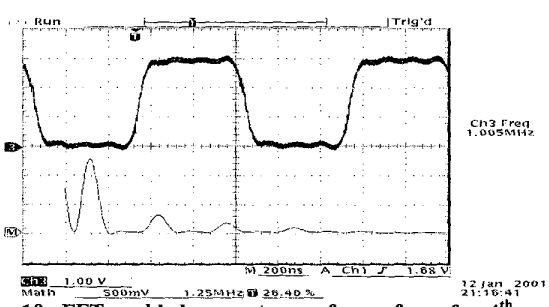

Fig. 10: FFT-enabled scope trace of waveform for 4th–order driver at 1MHz

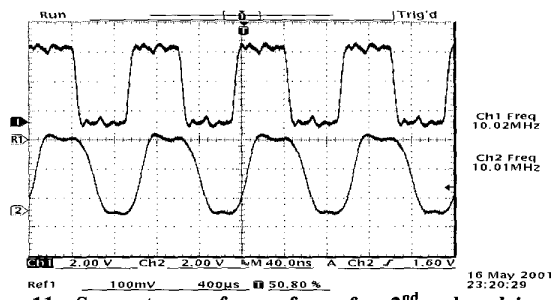

Fig. 11: Scope trace of waveform for 2nd-order driver at 10MHz

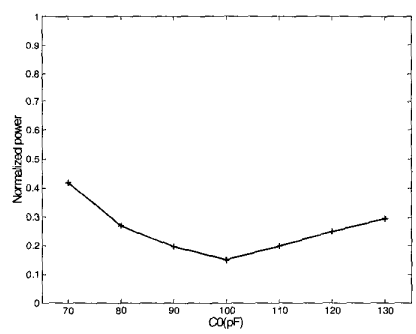

Fig. 12: Normalized power dissipation versus load capacitance. All components except load capacitance C_0 are kept same as designed for 100pF load capacitance.

6. CONCLUSION

In this paper, we presented a new algorithm and a prototype implementation of a harmonic resonant rail driver. The design goal was to produce an energy-efficient harmonic resonant clock signal using a simple network topology requiring no additional DC power supply. The experiment result shows that a significant energy for driving clock load can be recycled and saved by the

resonant characteristic of the proposed driver. Depending on the number of harmonics in the driver, we were able to save 70-85% of the conventional power dissipation. Moreover, the frequency variation caused by changes in load capacitance demonstrated significant improvement from the previously reported resonant clock drivers.

Application to two-phase requires more work. In particular, generating non-overlapping two-phase clocks using this driver is inherently impossible due to 50% duty cycle and relatively slow transition times for low-order drivers. One possible solution would be to drive a single-rail resonant rail driver shown in Fig. 1 by the proposed driver. This all-resonant rail driver has better energy efficiency than the single-rail driver and does not suffer from the load balancing issues of the blip driver. True single-phase energy-recovery logic [9] is another possible application for the proposed driver as we can adjust the clock waveform to closely simulate a voltage ramp rather than a sinusoidal clock signal. For single-phase low supply voltage system, the proposed driver can be directly applied for driving a clock network since the short-circuit current caused by the slow-edge of the clock signal becomes negligible as the supply voltage approaches $2V_{th}$ [10]. In addition, for high frequency applications, the proposed drivers' transition times of 10% of the total cycle time is sufficiently small to ensure nominal static power dissipation.

7. ACKNOWLEDGMENTS

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