Voltage-Pulse Driven Harmonic Resonant Rail Drivers for Low-Power Applications

Joong-Seok Moon, *Member, IEEE*, William C. Athas, *Member, IEEE*, Sigfrid D. Soli, Jeffrey T. Draper, *Member, IEEE*, and Peter A. Beerel, *Member, IEEE*

***Abstract*—We describe a new design technique for efficient harmonic resonant rail drivers. The proposed circuit implementation is coupled to a standard pulse source and uses only discrete passive components and no external dc power supply. It can thus be externally tuned to minimize the consumed power in the target IC. A new design technique based on current-fed voltage pulse-forming network theory is proposed to find the value of each discrete component for a target frequency and a given load capacitance. The proposed circuit topology can be used to generate any desired periodic 50% duty-cycle waveform by superimposing multiple harmonics of the desired waveform, however, this paper focuses on the generation of trapezoidal-wave clock signals. We have tested the driver with a capacitive load between 38.3 and 97.8 pF with clock frequency ranging between 0.8 and 15 MHz. The overall power dissipation for our second-order harmonic rail driver is 19% of fC_LV^2 at 15 MHz and 97.8 pF load.**

***Index Terms*—Clock generator, energy-recovery circuit, harmonic resonance, low power.**

I. Introduction

LOW POWER has become a critical feature of many CMOS-VLSI systems because of the increasing demand for a longer battery life and the high costs of heat removal. Because clocking circuitry is typically a significant source of power dissipation [1], reducing the power consumed by clock drivers and clock nets has become an important focus. Because clock nets are mostly capacitive, resonant charging techniques that recycle most of the energy stored in clock nets are increasingly promising. The simplest resonant charging technique uses the flyback circuit shown in Fig. 1 to generate a sinusoidal clock signal [2]. Although simple, if the nMOS transistor is driven nonresonantly, which has generally been the case, the energy efficiency of this clock driver is poor. The blip circuit [3], illustrated in Fig. 2, has much higher efficiency because it is all-resonant, i.e., the energy used to drive every transistor is recycled. This circuit successfully has been used as an efficient power source for drivers of large on-chip signal lines of microprocessors [2], [4] but can also be used to generate two-phase almost-nonoverlapping sinusoidal clocks.

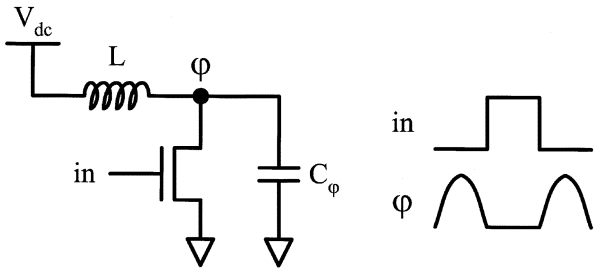


Fig. 1. Single-rail resonant clock driver (flyback circuit).

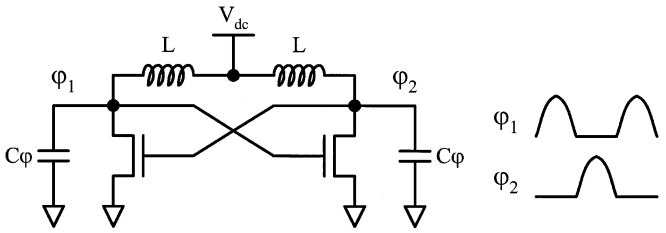


Fig. 2. All-resonant blip driver.

A common disadvantage of both these clock drivers is that the output signal frequency and magnitude depend heavily on the load capacitances $C\varphi$. Because the value of $C\varphi$ may be data-dependent and can thus vary from cycle to cycle, the clock frequency may also fluctuate, thereby decreasing performance and increasing design effort [5]. Of the two drivers, the frequency fluctuation in the blip driver is more pronounced because of the positive-feedback nature of the two outputs. Another disadvantage of both of these drivers is the need for a distinct dc power supply $V_{\rm dc}$ whose value is determined by the load capacitance and the target frequency.

Lastly, while sinusoidal clock signals are well-suited for special *adiabatic* circuits [6], [7], the slow slew rates cause two problems for conventional clock nets. In particular, while adiabatic circuits have special circuitry that prevents the slow slew rates from causing high short-circuit current, conventional clock buffers, flip-flops, and latches do not have these features and thus, have relatively fast clock slew rate requirements. Secondly, slow slew rates cause increased variations on effective clock skew and clock-output delay which may considerably affect potential performance and system stability.

Manuscript received February 28, 2002; revised September 20, 2002. This work was supported in part by the House Ear Institute under Grant PHS-398, in part by DARPA under Grant F30602-98-2-0108, and in part by the National Science Foundation ITR Award.

J.-S. Moon was with Information Sciences Institute, University of Southern California, Marina del Rey, CA 90292 USA. He is now with Apple Computer Inc., Cupertino, CA 95014 USA (e-mail: jsmoon@apple.com; athas@apple.com).

S. D. Soli is with House Ear Institute, Los Angeles, CA 90057 USA (e-mail: ssoli@hei.org).

J. T. Draper is with the Information Sciences Institute, University of Southern California, Marina del Rey, CA 90292 USA (e-mail: draper@isi.edu).

W. C. Athas is with Apple Computer Inc., Cupertino, CA 95014 USA (e-mail: athas@apple.com).

P. A. Beerel is with University of Southern California, Los Angeles, CA 90089 USA (e-mail: pabeerel@usc.edu).

Digital Object Identifier 10.1109/TVLSI.2003.814323

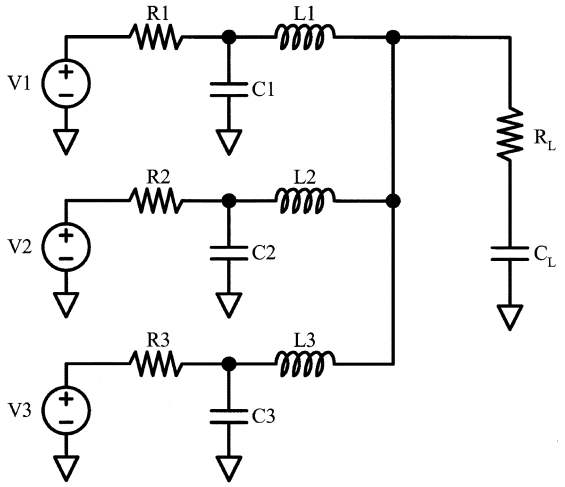


Fig. 3. Harmonic resonant rail driver containing three harmonic terms.

Younis and Knight [8] developed an incremental design approach for a class of efficient harmonic rail drivers that solves these problems. Their drivers approximate a desired square wave (with 50% duty cycle) by superpositioning its first n harmonics, as illustrated by the third-order driver in Fig. 3. These drivers, however, require n distinct dc power supplies, which is prohibitive for most practical implementations.

In this paper, we present a new systematic design approach for nth-order harmonic resonant rail drivers that do not require additional dc power supplies. Linear network theory is normally applied to predict the waveform generated by a network of passive components. Our design approach applies it for the inverse problem. That is, we use linear network theory to systematically derive a network of passive components that generates nth-order approximations of any given desired clock waveform with 50% duty cycle that can be expressed as a periodic trapezoid. In this way, we can achieve approximations of both ideal square waves and more practical waveforms with finite rise and fall times. In particular, we use linear network theory to develop a noniterative method for calculating the component values given the desired waveform shape and the nominal value of the load capacitance.

The topology of our proposed driver is based on a modified current-fed voltage pulse-forming network (CFVPN) [9]. This network is traditionally connected to a constant current source, which internally consumes significant power. In contrast, we propose using a conventional pulse generator that consumes much less internal power and is readily available in most systems. Moreover, it requires no additional distinct dc voltage/current supply and reduces the impact of variations in load capacitance on fluctuations in output magnitude and frequency. Self-oscillating resonant circuits such as flyback and blip circuits cannot be trivially synchronized to an external clock signal connected to other blocks in the system. However, this can be easily achieved in our design because it is driven by an external pulse generator.

Our proposed design approach has been implemented and tested for frequencies up to 15 MHz with various load capacitances. The worst case overall power dissipation of the second-order driver is 19% of fC_LV^2 at 15 MHz with a 97.8-pF load. Magnitude and frequency fluctuation due to a broad range of load capacitances variation are observed to be minimal. In addition, the power efficiency as a function of load capacitance and input pulse frequency variations is quantified.

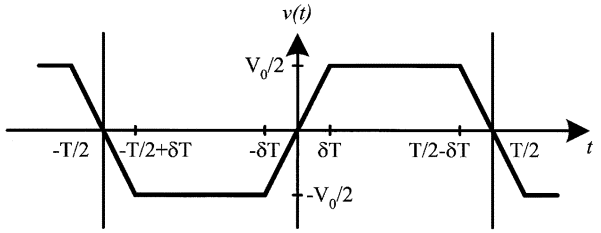


Fig. 4. Trapezoidal-wave voltage signal with slope $V_0/(2^*\delta T)$.

The remainder of this paper is organized as follows. In Section II, we briefly review the theory of waveform synthesis using current-fed voltage pulse-forming networks. Section III describes our systematic approach to identify the value of all driver components. Then, Section IV discusses practical implementations, Section V presents laboratory measurement results, and Section VI concludes with a discussion of potential applications and future work.

II. Current-Fed Voltage Pulse-Forming Network

This section reviews standard implementations of Fourier series approximations of periodic trapezoidal waveforms using current-fed voltage pulse-forming networks.

A trapezoidal wave $v(t)$, shown in Fig. 4, can be defined by the following:

$$v(t) = \begin{cases} \dfrac{V_0}{2}\dfrac{t}{\delta T}, & 0 \le t \le \delta T \\ \dfrac{V_0}{2}, & \delta T \le t \le T/2 - \delta T \\ \dfrac{V_0}{2}\dfrac{T/2 - t}{\delta T}, & T/2 - \delta T \le t \le T/2 \end{cases}$$

$$v(t) = -v(-t)$$

$$v(t + kT) = v(t), \qquad \text{where } k \text{ is integer.} \tag{1}$$

Because the trapezoidal waveform $v(t)$ is an odd function, the Fourier series for $v(t)$ contains only sine terms as follows:

$$v(t) = \sum_{k=1,\,3,\,\ldots}^{\infty} b_k \sin\frac{2\pi k t}{T} \tag{2}$$

where

$$b_k = \frac{4}{T}\int_0^{T/2} v(t)\sin\frac{2\pi k t}{T}\,dt = \frac{2V_0}{k\pi}\frac{\sin 2\pi k\delta}{2\pi k\delta}, \qquad \text{where } k = 1, 3, \ldots. \tag{3}$$

In practice, only the first few terms are needed to yield a waveform that closely approximates an ideal trapezoidal wave. Notice that the model approximates a square wave as δ becomes zero.

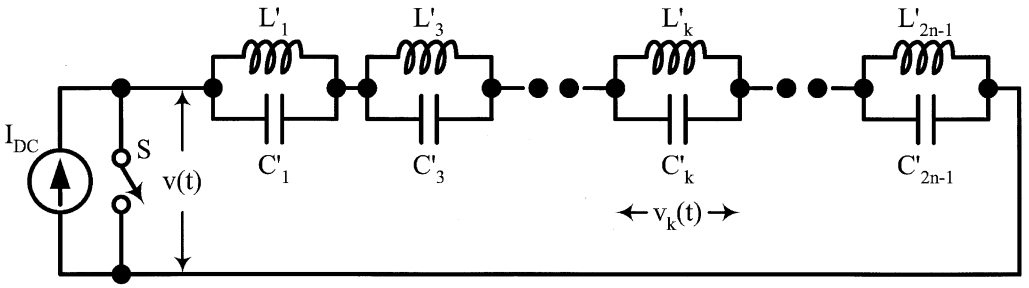


Fig. 5. CFVPN.

A CFVPN that can generate an output voltage $v(t)$ consisting of the superposition of n harmonics is shown in Fig. 5 [9]. To analyze $v(t)$, first assume that switch S opens at $t = 0$ and there is no energy initially stored in the network. The voltage across the kth LC section is shown in (4)

$$v_k(t) = I_{dc}\sqrt{\frac{L'_k}{C'_k}}\ \sin\ \frac{t}{\sqrt{L'_k C'_k}}. \tag{4}$$

Cascading n such LC sections in series yields the following for $v(t)$:

$$v(t) = \sum_{k=1,\,3,\,\ldots}^{2n-1} I_{dc}\sqrt{\frac{L'_k}{C'_k}}\ \sin\ \frac{t}{\sqrt{L'_k C'_k}}. \tag{5}$$

With this analysis, it is straightforward to determine the values of all network components to approximate a trapezoidal waveform defined by (2) and (3). In particular, by comparing (5) with (2), the values of b_k, L'_k, and C'_k for both square and trapezoidal waveforms can be easily determined, as summarized in Table I. As is, however, this network cannot be directly used as a clock rail driver because none of the capacitances in the network represents a load capacitance that resides between the output node and ground. To meet this requirement, an equivalent network can be derived through mathematical transformations of impedance and admittance functions of the output, as shown in the following:

$$Z(s) = \sum_{k=1,\,3,\,\ldots}^{2n-1} \frac{L'_k s}{L'_k C'_k s^2 + 1} \tag{6}$$

$$Y(s) = \frac{1}{Z(s)} = \frac{\prod_{k=1,3,\ldots}^{2n-1}(L'_k C'_k s^2 + 1)}{\sum_{k=1,3,\ldots}^{2n-1} L'_k s \prod_{\substack{i=1,3,\ldots \\ i\neq k}}^{2n-1}(L'_i C'_i s^2 + 1)}. \tag{7}$$

Notice that the impedance function $Z(s)$ has zeros at $s = 0$ and $s = \infty$, which in turn appear as poles in the admittance function $Y(s)$. We, therefore, can rewrite (7) as follows:

$$Y(s) = \frac{A_0}{s} + A_n s + \sum_{k=1}^{n-1} \frac{A_k s}{B_k s^2 + 1} \tag{8}$$

TABLE I
COMPONENT VALUES FOR NETWORK OF FIG. 5

	Square-Wave	Trapezoidal
b_k	$\frac{2V_0}{k\pi}$	$\frac{2V_0}{k\pi}\frac{\sin 2\pi k\delta}{2\pi k\delta}$
L_k	$\frac{V_0 T}{\pi^2 k^2 I_{DC}}$	$\frac{V_0 T}{\pi^2 k^2 I_{DC}}\left(\frac{\sin 2\pi k\delta}{2\pi k\delta}\right)$
C_k	$\frac{I_{DC} T}{4V_0}$	$\frac{I_{DC} T}{4V_0}\left(\frac{\sin 2\pi k\delta}{2\pi k\delta}\right)^{-1}$

where

$$A_0 = \frac{1}{L_0}, \qquad A_n = C_L, \qquad A_k = C_k, \qquad B_k = C_k L_k \tag{9}$$

and the values for C_L and L_0 are determined as follows:

$$L_0 = \frac{1}{A_0} = \lim_{s\to 0}\frac{1}{Y(s)s} = \lim_{s\to 0}\frac{Z(s)}{s} = \sum_{k=1,\,3,\,\ldots}^{2n-1} L'_k$$

$$\frac{1}{C_L} = \frac{1}{A_n} = \lim_{s\to\infty}\frac{s}{Y(s)} = \lim_{s\to\infty} sZ(s) = \sum_{k=1,\,3,\,\ldots}^{2n-1}\frac{1}{C'_k}. \tag{10}$$

This transformation enables $Y(s)$ to be generated using the alternative circuit topology illustrated in Fig. 6, which is now suitable as a clock rail driver because it has an explicit clock load capacitance C_L that lies between the output and ground.

To find the values of other components of Fig. 6, we can use a partial fraction expansion of the admittance function $Y(s)$ [10], which is an iterative numerical procedure that provides little insight into the operation of the network. In Section III, we present a characteristic equation that constrains component values so that only desired frequency components are produced in the network and together with a set of linear equations provides a more insightful closed-form expression for component values.

III. THEORETICAL ANALYSIS OF CFVPN

There are three steps in our theoretical and algorithmic analysis of the CFVPN and its desired component values. First, we convert all of node voltage and branch current equations from time-domain to frequency-domain using the Laplace transform. Second, the branch current equations are simplified to find a

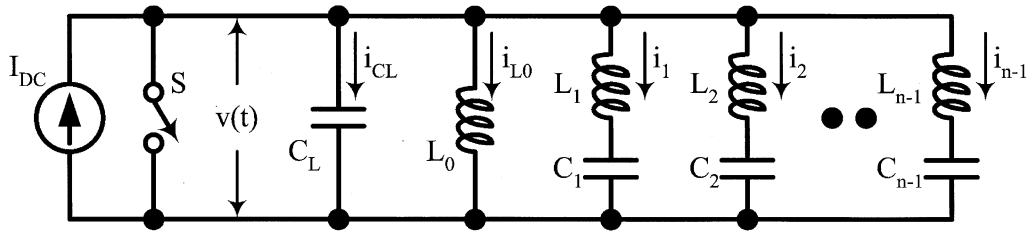


Fig. 6. An equivalent network of Fig. 5 containing a capacitance C_L that can represent an on-chip clock load.

characteristic equation whose roots are the product of L_k and C_k of each branch such that all unwanted frequency components are suppressed. Using these roots, the third step is to establish a set of linear equations that can be found by applying KCL on the output node to identify all of the inductor values in the network. These values are combined with the roots of the characteristic equation to identify all of the capacitor values.

A. Step 1: Convert Voltage and Current Equations to Frequency-Domain Representation

To ease the tedium and complexity of solving the integral and differential equations, we use the Laplace transform to convert voltage and current equations into the frequency domain. Since two networks shown in Figs. 5 and 6 are equivalent, we write the Laplace transform of the output voltage $v(t)$ of Fig. 6 by approximating (2) to the nth order, i.e.,

$$V(s) = \omega_0 \left(\frac{b_1}{s^2+\omega_0^2} + \cdots + \frac{b_{2n-1}(2n-1)}{s^2+(2n-1)^2\omega_0^2} \right) \quad \text{where } \omega_0 = \frac{2\pi}{T}. \tag{11}$$

By noting that voltages across all of the branches in Fig. 6 equal $v(t)$, it is straightforward to derive the Laplace transform for each branch current as follows:

$$I_{C_L}(s) = C_L\omega_0 \left(\frac{b_1 s}{s^2+\omega_0^2} + \cdots + \frac{b_{2n-1}(2n-1)s}{s^2+(2n-1)^2\omega_0^2} \right) \tag{12}$$

$$I_{L0}(s) = \frac{\omega_0}{L_0} \left(\frac{b_1}{s(s^2+\omega_0^2)} + \cdots + \frac{b_{2n-1}(2n-1)}{s(s^2+(2n-1)^2\omega_0^2)} \right) = \frac{1}{L_0\omega_0} \sum_{j=1}^{n} \frac{b_{2j-1}}{(2j-1)} \left(\frac{1}{s} - \frac{s}{s^2+(2j-1)^2\omega_0^2} \right) \tag{13}$$

$$I_k(s) = \frac{1}{L_k} \frac{s}{s^2+\frac{1}{L_kC_k}} V(s) = \frac{\omega_0}{L_k} \frac{s}{s^2+\Omega_k^2} \left(\frac{b_1}{s^2+\omega_0^2} + \cdots + \frac{b_{2n-1}(2n-1)}{s^2+(2n-1)^2\omega_0^2} \right) \tag{14}$$

where

$$\Omega_k = 1 \Big/ \sqrt{L_kC_k}\,, \qquad \text{for } 1 \le k \le n-1. \tag{15}$$

B. Step 2: Simplify Branch Current Equations and Establish the Characteristic Equation

As shown in (14), each branch introduces a new free oscillation frequency component at Ω_k. This frequency component is unwanted because the output of the network should have only n desired harmonics at ω_0 to $(2n-1)\omega_0$. By simplifying the branch current equation and finding a condition to suppress the frequency component at Ω_k, we can establish the characteristic equation whose roots are $n-1$ distinct Ω_k values and thus, the product of L_k and C_k.

To simplify the branch current equation, we can rewrite (14) as follows:

$$\begin{aligned} I_k(s) &= \frac{\omega_0}{L_k} \frac{s}{s^2+\Omega_k^2} \left(\frac{b_1}{s^2+\omega_0^2} + \cdots + \frac{b_{2n-1}(2n-1)}{s^2+(2n-1)^2\omega_0^2} \right) \\ &= \frac{\omega_0}{L_k} \left(\frac{A_{k1}s}{s^2+\Omega_k^2} + \frac{B_{k1}s}{s^2+\omega_0^2} + \cdots + \frac{A_{kn}s}{s^2+\Omega_k^2} + \frac{B_{kn}s}{s^2+(2n-1)^2\omega_0^2} \right). \end{aligned} \tag{16}$$

By comparing jth terms, two conditions for A_{kj} and B_{kj} can be found

$$\frac{b_{2j-1}(2j-1)s}{(s^2+\Omega_k^2)(s^2+(2j-1)^2\omega_0^2)} = \frac{A_{kj}s}{s^2+\Omega_k^2} + \frac{B_{kj}s}{s^2+(2j-1)^2\omega_0^2} \tag{17}$$

$$\begin{aligned} & b_{2j-1}(2j-1)s \\ &= (A_{kj}+B_{kj})s^3 + (A_{kj}(2j-1)\omega_0^2 + B_{kj}\Omega_k^2)s \\ &\therefore \quad \begin{aligned} & A_{kj}+B_{kj} = 0 \\ & A_{kj}(2j-1)^2\omega_0^2 + B_{kj}\Omega_k^2 = b_{2j-1}(2j-1). \end{aligned} \end{aligned} \tag{18}$$

Equation (16) can now be simplified by replacing B_{kj} with $-A_{kj}$ and collecting the Ω_k terms together

$$\begin{aligned} I_k(s) &= \frac{\omega_0}{L_k} \left(\frac{A_{k1}s}{s^2+\Omega_k^2} + \frac{-A_{k1}s}{s^2+\omega_0^2} + \cdots + \frac{A_{kn}s}{s^2+\Omega_k^2} + \frac{-A_{kn}s}{s^2+(2n-1)^2\omega_0^2} \right) \\ &= \frac{\omega_0}{L_k} \left(\frac{(A_{k1}+A_{k2}+\cdots+A_{kn})s}{s^2+\Omega_k^2} + \frac{-A_{k1}s}{s^2+\omega_0^2} + \cdots + \frac{-A_{kn}s}{s^2+(2n-1)^2\omega_0^2} \right). \end{aligned} \tag{19}$$

By applying KCL on the output node of the network, the relationship of branch currents can be defined by

$$\sum_{k=1}^{n-1} I_k(s) = \frac{I_{dc}}{s} - I_{C0}(s) - I_{L0}(s). \tag{20}$$

Because no Ω_k term exists in the right side of this equation, the Ω_k term in each branch current must evaluate to zero, implying the following additional constraint

$$\sum_{j=1}^{n} A_{kj} = 0. \tag{21}$$

Equations (18) and (21) are combined to produce the characteristic equation shown in (23),

$$\begin{aligned} A_{kj}((2j-1)^2\omega_0^2 - \Omega_k^2) &= b_{2j-1}(2j-1) \\ A_{kj} &= \frac{b_{2j-1}(2j-1)}{(2j-1)^2\omega_0^2 - \Omega_k^2} \\ &= \frac{2V_0}{\pi} \frac{\sin 2\pi(2j-1)\,\delta}{2\pi(2j-1)\,\delta} \frac{1}{(2j-1)^2\omega_0^2 - \Omega_k^2} \qquad (22) \\ \sum_{j=1}^{n} A_{kj} &= \frac{2V_0}{\pi\omega_0^2} \sum_{j=1}^{n} \frac{\sin 2\pi(2j-1)\,\delta}{2\pi(2j-1)\,\delta} \frac{1}{(2j-1)^2 - x} = 0 \\ &\text{where } x = \left(\frac{\Omega_k}{\omega_0}\right)^2. \qquad (23) \end{aligned}$$

Notice that the numerator of the characteristic equation is an order-$(n-1)$ polynomial of variable x. The roots of this numerator polynomial, α_1 to α_{n-1}, are the roots of the entire characteristic equation, which can be represented as follows:

$$\alpha_1 = \frac{\Omega_1^2}{\omega_0^2}, \quad \alpha_2 = \frac{\Omega_2^2}{\omega_0^2}, \ldots, \alpha_{n-1} = \frac{\Omega_{n-1}^2}{\omega_0^2}. \tag{24}$$

C. Step 3: Setup Linear Equations to Find a Set of L_k and Combine With the Roots of the Characteristic Equation to Find a Set of C_k

Using (24), we can substitute Ω_k^2 with the product α_k and ω_0^2 in (22) and use the result to simplify (20) as follows:

$$\begin{aligned} \frac{I_{\rm dc}}{s} - I_{C_L}(s) &= I_{L0}(s) + \sum_{k=1}^{n-1} I_k(s) \\ \frac{I_{\rm dc}}{s} - C_L\omega_0 \left(\frac{b_1 s}{s^2+\omega_0^2} + \cdots + \frac{b_{2n-1}(2n-1)s}{s^2+(2n-1)^2\omega_0^2}\right) &= \frac{1}{L_0\omega_0}\left(b_1 + \frac{b_3}{3} + \cdots + \frac{b_{2n-1}}{(2n-1)}\right)\frac{1}{s} - \frac{b_1}{\omega_0}\frac{s}{s^2+\omega_0^2} \\ &\quad \times \left(\frac{1}{L_0} + \frac{1}{(1-\alpha_1)L_1} + \cdots + \frac{1}{(1-\alpha_{n-1})L_{n-1}}\right) \\ &\quad - \frac{3b_3}{\omega_0}\frac{s}{s^2+3^2\omega_0^2} \\ &\quad \times \left(\frac{1}{3^2L_0} + \frac{1}{(3^2-\alpha_1)L_1} + \cdots + \frac{1}{(3^2-\alpha_{n-1})L_{n-1}}\right) \\ &\quad - \cdots - \frac{(2n-1)b_{2n-1}}{\omega_0}\frac{s}{s^2+(2n-1)^2\omega_0^2} \\ &\quad \times \left(\frac{1}{(2n-1)^2L_0} + \cdots + \frac{1}{((2n-1)^2-\alpha_{n-1})L_{n-1}}\right). \end{aligned} \tag{25}$$

Comparing both sides of (25), the linear equations shown in (26) determine the inductor values $L_1, \ldots, L_{n-1}$. Note that these values can be combined with (24) to calculate the capacitance values $C_1, \ldots, C_{n-1}$

$$\begin{bmatrix} 1 & \frac{1}{1-\alpha_1} & \cdots & \frac{1}{1-\alpha_{n-1}} \\ \frac{1}{3^2} & \frac{1}{3^2-\alpha_1} & \cdots & \frac{1}{3^2-\alpha_{n-1}} \\ \cdots & \cdots & \cdots & \cdots \\ \frac{1}{(2n-1)^2} & \frac{1}{(2n-1)^2-\alpha_1} & \cdots & \frac{1}{(2n-1)^2-\alpha_{n-1}} \end{bmatrix} \times \begin{bmatrix} \frac{1}{L_0} \\ \frac{1}{L_1} \\ \cdots \\ \frac{1}{L_{n-1}} \end{bmatrix} = C_L\omega_0^2 \begin{bmatrix} 1 \\ 1 \\ \cdots \\ 1 \end{bmatrix}. \tag{26}$$

As an example, consider the task of finding the value of all components of the second-order square-wave driver for a 1-MHz clock and a 100-pF load. From (23), we have

$$\begin{aligned} \frac{1}{1-x} + \frac{1}{9-x} &= 0 \\ \therefore x = \alpha_1 &= 5. \end{aligned} \tag{27}$$

Using this value, we can rewrite (26) as follows:

$$\begin{bmatrix} 1 & \frac{1}{1-5} \\ \frac{1}{3^2} & \frac{1}{3^2-5} \end{bmatrix} \begin{bmatrix} \frac{1}{L_0} \\ \frac{1}{L_1} \end{bmatrix} = 100 \times 10^{-12} \left(\frac{2\pi}{10^{-6}}\right)^2 \begin{bmatrix} 1 \\ 1 \end{bmatrix}. \tag{28}$$

By solving these equations, we find inductor values, $L_0 = 140.72$ uH and $L_1 = 79.16$ uH. Lastly, since $\Omega_1^2 = 5\omega_0^2 = 1/L_1C_1$, it follows that $C_1 = 64$ pF.

IV. Voltage-Pulse Driven Pulse-Forming Network

Even though the CFVPN shown in Fig. 6 has an appropriate configuration for our target applications, two problems preclude the network from being directly applied as a clock rail driver. First, a dc current source is required to drive the network that in practice consumes large amounts of power internally, canceling out the benefits of the CFVPN clock rail driver. Second, the waveform swings between $+V_0/2$ and $-V_0/2$ as opposed to 0 and $+V_0$ required for driving CMOS clock nets. We propose a unique solution that overcomes these impediments.

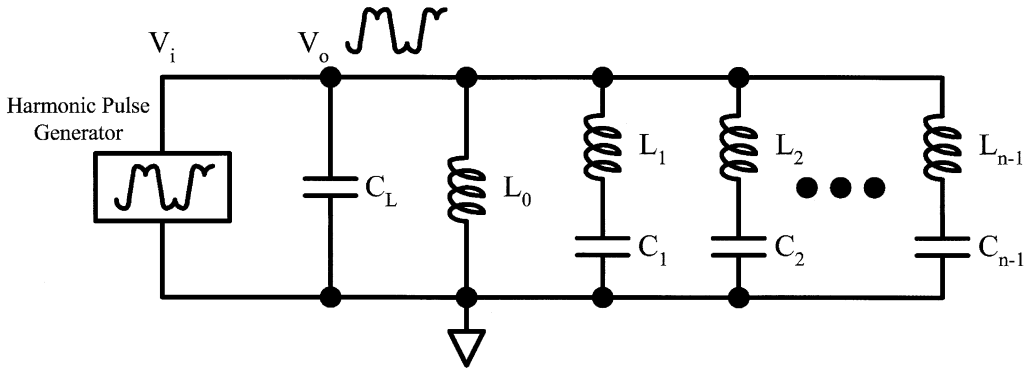


Fig. 7. Equivalent network of Fig. 6 driven by a voltage pulse.

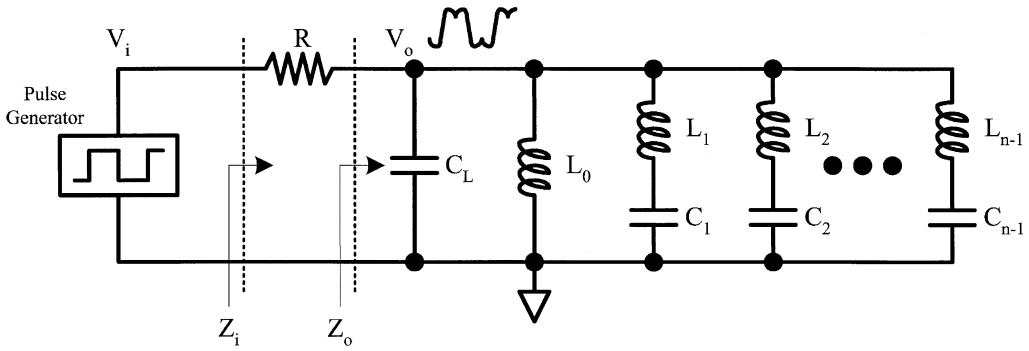


Fig. 8. Practical approximation of the network shown in Fig. 7.

A. Voltage-Pulse Driven Network for dc Current Source Elimination

In theory, to eliminate the dc current source of the CFVPN we can use the equivalent network shown in Fig. 7, which is triggered by a voltage source generating a waveform identical to the desired output that provides no current, and thus consumes no power. However, it is impractical to build a voltage source that generates a waveform matching the desired nth-order harmonic voltage waveform. Thus, we propose a solution that uses a more practical voltage pulse whose undesired harmonics are effectively absorbed using a series resistor.

The cheapest source of the voltage pulses is a conventional clock oscillator that, given finite rise and fall times, approximates a trapezoidal wave. The first n harmonics of the trapezoidal waveform should match that of the network. However, the trapezoidal-wave clock signal will also contain higher order harmonics than those generated by the network. This will cause significant current draw from the voltage source, reducing the power efficiency of the proposed rail driver.

We propose to reject these higher order harmonics from the input pulse generator by placing a resistor between the input and output of the network as depicted in Fig. 8. To understand the benefits of adding this resistor we first write the impedance function of the original network as follows:

$$Z_o(j\omega) = \frac{j\omega L_1'}{1-\omega^2/\omega_0^2} + \frac{j\omega L_3'}{1-\omega^2/3^2\omega_0^2} + \cdots + \frac{j\omega L_{2n-1}'}{1-\omega^2/(2n-1)^2\omega_0^2}. \quad (29)$$

Note that (29) is the impedance function of the network shown in Fig. 5 that is the equivalent network of Fig. 6. Then, by adding the resistance R, the overall impedance seen by the input pulse generator is

$$\begin{aligned} Z_i(j\omega) &= R + Z_o(j\omega) \\ &= R + \frac{j\omega L_1'}{1-\omega^2/\omega_0^2} + \frac{j\omega L_3'}{1-\omega^2/3^2\omega_0^2} + \cdots \\ &\quad + \frac{j\omega L_{2n-1}'}{1-\omega^2/(2n-1)^2\omega_0^2}. \end{aligned} \quad (30)$$

The transfer function $A(j\omega)$ of the network, represented as the ratio of impedance $Z_i(j\omega)$ and $Z_o(j\omega)$, is as follows:

$$\begin{aligned} \frac{V_o(j\omega)}{V_i(j\omega)} &= A(j\omega) = \frac{Z_o(j\omega)}{Z_i(j\omega)} \\ &= \frac{\frac{j\omega L_1'}{1-\omega^2/\omega_0^2} + \cdots + \frac{j\omega L_{2n-1}'}{1-\omega^2/(2n-1)^2\omega_0^2}}{R + \frac{j\omega L_1'}{1-\omega^2/\omega_0^2} + \cdots + \frac{j\omega L_{2n-1}'}{1-\omega^2/(2n-1)^2\omega_0^2}} \\ &= \frac{jz_0}{R+jz_0}, \qquad \text{where } z_0 \text{ is real} \end{aligned} \quad (31)$$

where $Z_o(j\omega) = jz_0(\omega)$. The magnitude and phase shift of this transfer function can then be expressed as follows:

$$\begin{aligned} |A(j\omega)| &= \frac{|z_0|}{\sqrt{R^2+z_0^2}} \\ \angle A(j\omega) &= \angle jz_0 - \angle(R+jz_0). \end{aligned} \quad (32)$$

Thus, for all frequencies other than the harmonic frequencies (where z_0 is finite), the magnitude approaches zero and the

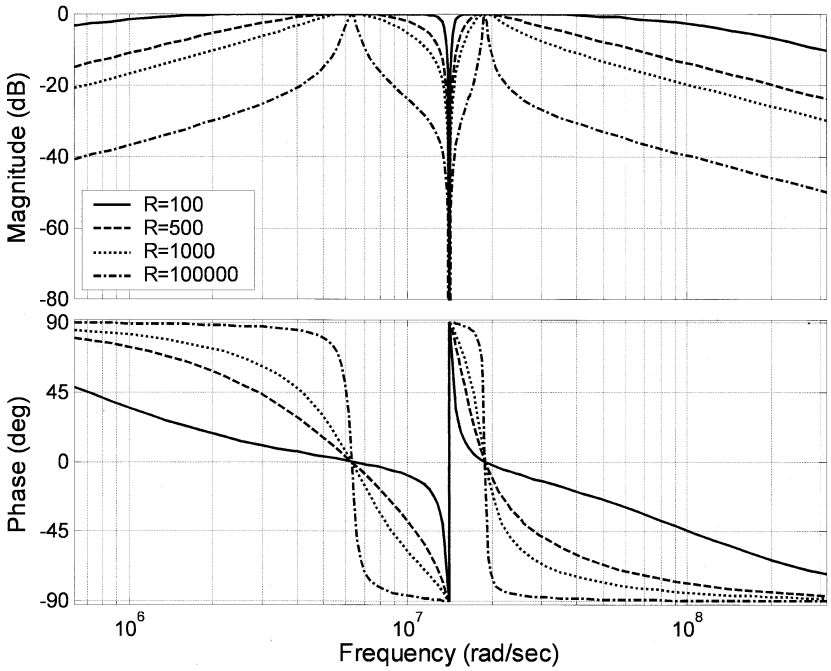


Fig. 9. Frequency response of the network shown in Fig. 8 $(V_o(s)/V_i(s))$.

phase shift approaches 90° as the value of R increases. Moreover, the magnitude and phase of the transfer function at each of the n harmonic frequencies can be calculated as follows:

$$A(j\omega_k) = \lim_{z_0 \to \infty} \frac{jz_0}{R + jz_0}$$

$$|A(j\omega_k)| = \lim_{z_0 \to \infty} \frac{|z_0|}{\sqrt{R^2 + z_0^2}} = 1$$

$$\angle A(j\omega_k) = \angle j\infty - \angle(R + j\infty) = \pi/2 - \pi/2 = 0 \quad (33)$$

where $\omega_k = (2k-1)\omega_0$ for $k = 1, 2, \ldots, n$. Thus, the value of R does not affect the phase or magnitude of any of the generated harmonics. A more detailed analytical proof of (33) for the second-order driver example is presented in the Appendix. Fig. 9 depicts the frequency response of the second-order driver for a 1-MHz clock signal with different resistance values. It clearly shows that no distortion is incurred at two resonant frequencies (1 and 3 MHz) for all resistance values. From this graph, it seems beneficial to increase the resistance to reject higher harmonics. However, the parasitic resistances of the components and wires unfortunately reduce the voltage level of the output signal as R becomes larger because of the inherent voltage divider present between the parasitic resistances and R. To understand this more clearly, the driver is redrawn in Fig. 10 with a parasitic dc resistor associated with each inductor for the second-order. Other parasitic components whose values are negligible compared with components used are not considered to simplify the analysis. If we apply KCL on the output node, we can write the following:

$$\frac{V_i(s) - V_o(s)}{R} = \left(sC_L + \frac{1}{sL_0 + R_0} + \frac{sC_1}{s^2 L_1 C_1 + sR_1 C_1 + 1} \right) \cdot V_o(s). \quad (34)$$

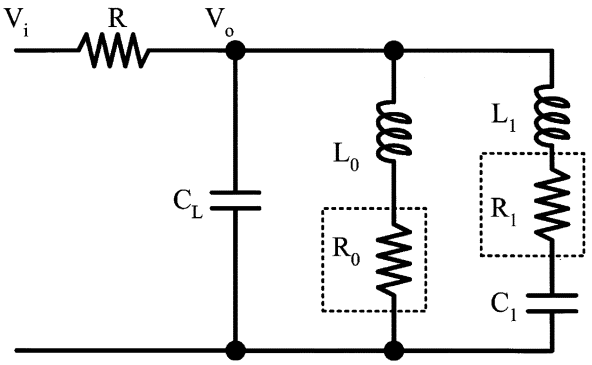
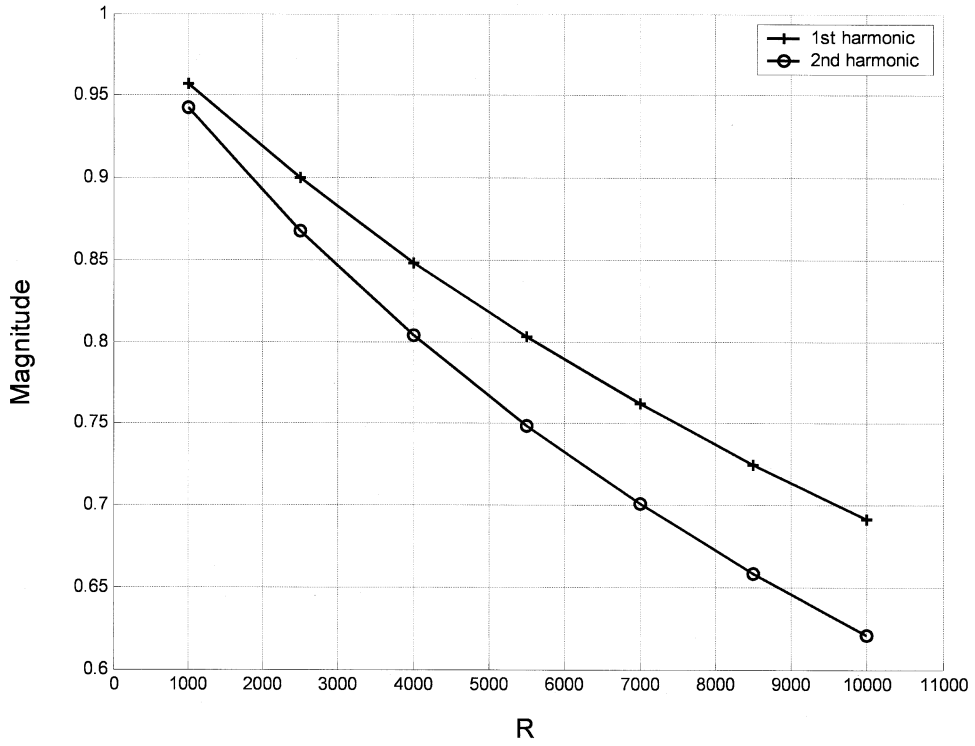


Fig. 10. Proposed network with the parasitic resistance of inductors.

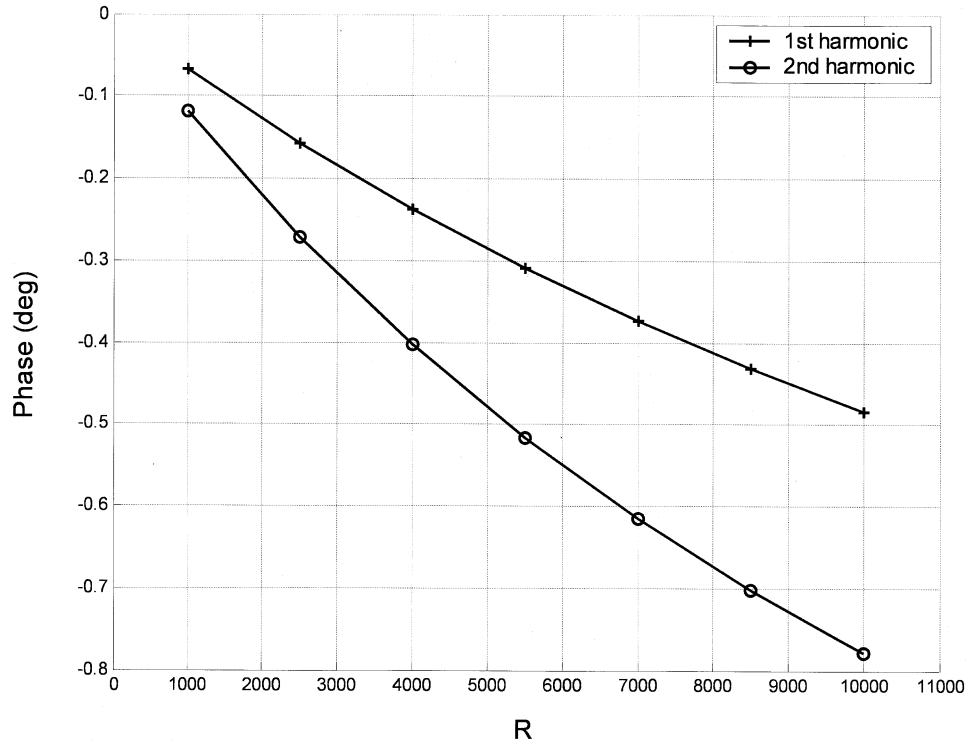
By arranging for V_o

$$V_o(s) = \frac{V_i(s)}{1 + sRC_L + \frac{R}{sL_0 + R_0} + \frac{sRC_1}{s^2 L_1 C_1 + sR_1 C_1 + 1}}. \quad (35)$$

Fig. 11 shows the magnitude and phase of V_i/V_o at the first two harmonic frequencies. $R_0 = 30\ \Omega$ and $R_1 = 25\ \Omega$ are used for the inductor parasitic resistances, as specified by the data sheet for the inductor used in our implementation [11]. Though there is negligible change in the phase, the magnitude decreases from 0.96 to 0.69 when R increases from 1 to 10 kΩ. This is in sharp contrast to the ideal network whose frequency response at the harmonic frequencies is not affected by the resistance value as demonstrated in Fig. 9. Consequently, it is important to use an adequate resistance value R while maintaining proper voltage levels of the output signal for low-power dissipation. For driving 97.8-pF load capacitance at 1 MHz, our test measurement demonstrates that only 15% of $fC_L V^2$ is dissipated with a 2-kΩ resistance with negligible degradation in output voltage.



(a)



(b)

Fig. 11. Frequency response of the network shown in Fig. 10 for the first two harmonic frequencies. (a) Magnitude (b) Phase.

B. A Tank Capacitor for a Positive-Swing Waveform

The output of the network in Fig. 8 swings between $+V_0/2$ and $-V_0/2$ because one branch between the output and ground contains a single inductor L_0. To redesign the network to swing from 0 to $+V_0$ we must introduce a dc offset to the output. We propose accomplishing this by introducing a dc offset at the pulse generator input and adding a tank capacitance C_T in series with L_0.

To understand how a dc offset from the input pulse generator affects the network, two circuits that differ only in an existence of C_T at the dc steady-state condition are shown in Fig. 12. Without C_T, the induced output dc voltage is zero because the

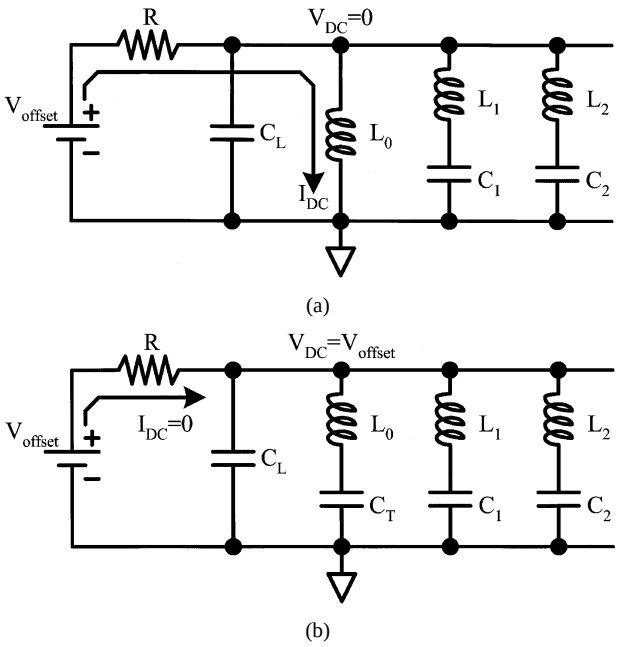


Fig. 12. dc steady-state for the network. (a) Without C_T. (b) With C_T.

output and ground node are shorted by the L_0 branch as shown in Fig. 12(a). As a result, the dc current V_{offset}/R flows into the network, creating significant unwanted dc power. For the network shown in Fig. 12(b), the tank capacitance C_T connected to L_0 in series induces a matching dc offset voltage at the output node, eliminating the dc current into the network.

Moreover, the introduction of the tank capacitor has a negligible impact on the overall frequency response of the rail driver. To see this, notice that the impedance functions for the branches in Fig. 12 that contain L_0 can be written as follows:

$$Z_1(j\omega) = j\omega L_0$$

$$Z_2(j\omega) = j\omega L_0 + \frac{1}{j\omega C_T} = j\,\frac{\omega^2 L_0 C_T - 1}{\omega C_T}. \qquad (36)$$

Assuming C_T is very large, the impedance of $Z_2(j\omega)$ is negligibly affected by C_T

$$Z_2(j\omega) = j\,\frac{\omega^2 L_0 C_T - 1}{\omega C_T} \approx j\,\frac{\omega^2 L_0 C_T}{\omega C_T} = j\omega L_0$$

$$Z_2(j\omega) \approx Z_1(j\omega), \qquad \text{when } \omega \gg \frac{1}{\sqrt{L_0 C_T}}. \qquad (37)$$

In our laboratory test, a 10 nF off-the-shelf capacitor was sufficient to achieve the desired dc offset voltage within an 0.8- to 15-MHz frequency range. The final proposed voltage-pulse driven positive-swing driver is shown in Fig. 13.

V. Measurement

The proposed harmonic resonant square-wave rail drivers containing up to four terms (i.e., fourth-order) were designed and tested on a wire-wrap board that included tunable inductors and capacitors. We varied the frequency from 0.8 to 15 MHz by setting these components to theoretical values we calculated using (23) and (26). We then tuned each component to achieve minimum measured power dissipation and compared them with their theoretical value. Testing at higher frequencies was limited by the test setup and equipments that are available to the authors.

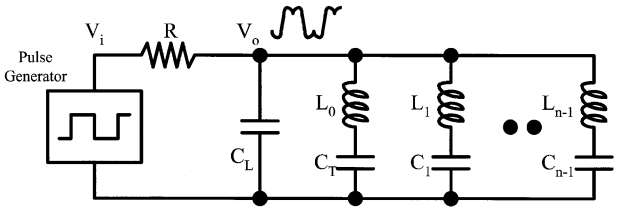


Fig. 13. Voltage-pulse driven harmonic resonant rail driver.

Table II summarizes the laboratory measurement results for various configurations. In most cases, the measured values of the components are within 7% of the theoretical values. Deviation between the theoretical and tuned capacitance values is larger than for the inductors presumably because of the large parasitic capacitances in our wire-wrapped board. As reported in Table II, approximately 19% of the calculated conventional power dissipation fC_LV^2 was dissipated for the second-order driver at 15 MHz to drive 97.8 pF load capacitance. Power dissipation increases as the order of the driver increases. This effect appears to be due to more parasitic components in the test board. In addition, tuning the circuit for minimum measured power dissipation is increasingly error prone since more design variables are involved. Note that as we increase the order of the driver, we must include additional capacitance such as $C1$ and $C2$ for the second-order driver. However, this does not increase the power dissipation significantly because only a small fraction of the current is drawn from the input pulse generator. In particular, the pulse generator needs to provide only a very small current sufficient to compensate the energy loss due to the parasitics of the components.

The last row in Table II shows the measurement data of the second-order driver for different load capacitances at 1 MHz. Resistance values are reduced to achieve 10% rising and falling times of the total cycle time. Power dissipation is increased by approximately 7% for this case while rising and falling times are shortened by 3% from the minimal power dissipation mode. This result suggests that by changing resistance value, we can control the rising and falling times at the expense of power dissipation. Fig. 14 illustrates the measured power dissipation as we changed the resistance value R for 1 MHz and 100 pF. The transition time with 2-kΩ resistance was measured as 110 ns, which is 11% of the total cycle time. Notice that transition times in Fig. 14 are normalized to this value. At 285 Ω, the transition time drops to 50 ns (45%) while the power dissipation increases from 15% to 57.9% of fC_LV^2.

Figs. 15 and 16 show oscilloscope traces of the output signal of the driver for the second- and third-order harmonics. To see how the output signal is synchronized, the input pulse is also shown. A fast Fourier (FFT)-enabled oscilloscope trace for the fourth-order driver output is presented in Fig. 17. The figure shows that only four harmonic frequencies are present in the output signal. Fig. 18 presents the trace of the output signal of the second-order harmonic driver for 10-MHz frequency.

When the driver is directly connected to the clock network, the nonlinear characteristic of the transistors can cause load capacitance variations. To measure power dissipation as

TABLE II
MEASURED DATA OF SECOND, THIRD, AND FOURTH SQUARE-WAVE HARMONIC RESONANT RAIL DRIVER FOR VARIOUS CLOCK FREQUENCIES AND LOAD CAPACITANCES. THE FIRST THREE ROWS ARE DATA FOR DRIVING 97.8 pF LOAD CAPACITANCE AT DIFFERENT CLOCK FREQUENCIES AND THE LAST ROW SHOWS DATA FOR DIFFERENT LOAD CAPACITANCES AT 1 MHz. THEORETICAL AND MEASURED VALUES OF EACH COMPONENT ARE ALSO SHOWN FOR COMPARISON

	f_{CLK} (MHz)	C_L	C1		C2		C3		L0		L1		L2		L3		R	P/fC_LV^2 (%)
			theory	measured	theory	measured	theory	measured	theory	measured	theory	measured	theory	measured	theory	measured		
	0.8	97.8	62.6	59.8	-	-	-	-	224.83	215.0	126.47	119.6	-	-	-	-	3.151	14.29
2^{nd}	1.0	97.8	62.6	59.8	-	-	-	-	143.89	135.9	80.94	75.6	-	-	-	-	2.015	14.53
order	2.0	97.8	62.6	59.0	-	-	-	-	35.97	34.6	20.23	18.8	-	-	-	-	1.183	14.88
V_H=3	5.0	97.8	62.6	59.3	-	-	-	-	5.76	5.6	3.24	2.96	-	-	-	-	0.493	14.66
V_L=0	10.0	97.8	62.6	56.0	-	-	-	-	1.44	1.50	0.81	0.79	-	-	-	-	0.120	16.58
	15.0	97.8	62.6	56.5	-	-	-	-	0.64	0.67	0.36	0.36	-	-	-	-	0.056	19.00
3^{rd}	0.8	97.8	105.3	98.8	21.4		-	-	155.28	155.2	81.49	80.3	98.84	94.8	-	-	2.311	16.45
order	1.0	97.8	105.3	99.5	21.4	19.5	-	-	99.38	99.7	52.15	50.7	63.26	61.8	-	-	1.671	16.61
V_H=3	2.0	97.8	105.3	100.1	21.4	19.4	-	-	24.84	24.3	13.04	12.6	15.81	15.3	-	-	0.879	16.78
V_L=0	5.0	97.8	105.3	103.5	21.4	19.3	-	-	3.98	3.9	2.09	1.9	2.53	2.3	-	-	0.353	17.48
4^{th}	0.8	97.8	146.4	137.0	33.2	30.8	11.7	10.2	118.53	117.5	60.86	60.8	66.68	67.0	83.15	78.0	1.417	26.41
order	1.0	97.8	146.4	138.3	33.2	30.4	11.7	9.9	75.86	76.6	38.95	39.8	42.68	43.8	53.22	50.0	0.958	28.03
V_H=3	2.0	97.8	146.4	138.0	33.2	31.4	11.7	9.9	18.96	19.2	9.74	9.7	10.67	10.7	13.30	12.0	0.617	27.16
V_L=0	5.0	97.8	146.4	138.2	33.2	31.8	11.7	10.3	3.03	2.9	1.56	1.5	1.71	1.6	2.13	2.1	0.223	28.52
2^{nd}	1.0	38.2	24.4	21.6	-	-	-	-	368.39	350.0	207.32	199.6	-	-	-	-	2.48	23.85
order	1.0	55.4	35.5	34.2	-	-	-	-	254.01	243.3	142.88	138.4	-	-	-	-	1.867	23.27
V_H=3	1.0	67.7	43.3	45.5	-	-	-	-	207.86	198.0	116.92	109.3	-	-	-	-	1.592	22.73
V_L=0	1.0	84.0	53.8	56.0	-	-	-	-	167.53	160.30	94.23	90.10	-	-	-	-	1.577	22.76

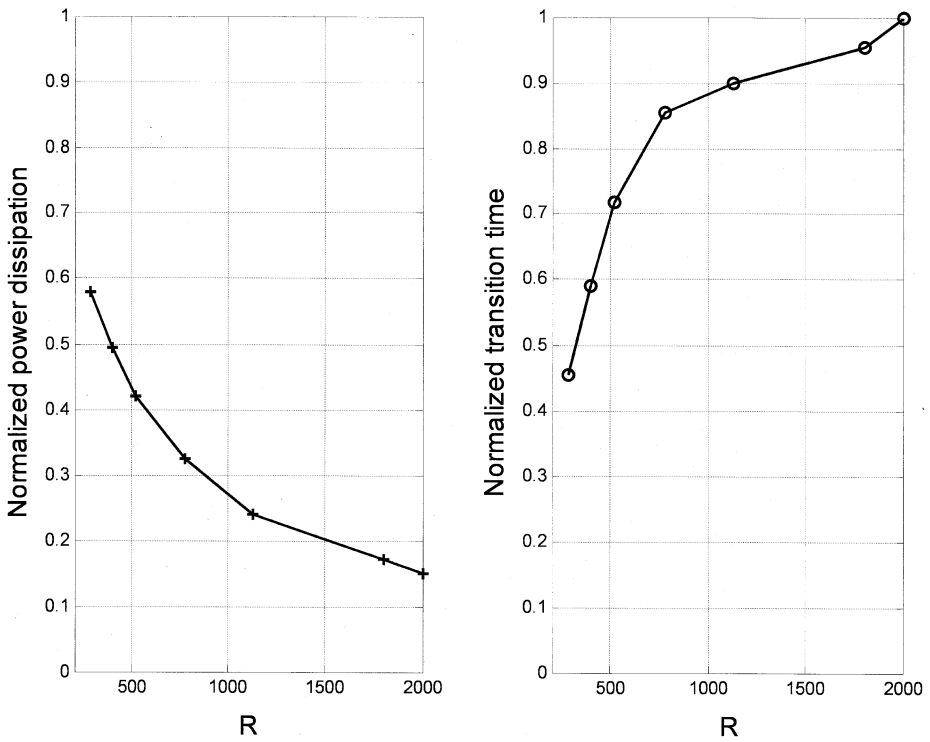


Fig. 14. Normalized power dissipation (P/fC_LV^2) and transition time versus resistance R. fC_LV^2 is the theoretical conventional power dissipation to drive load capacitance C_L.

a function of the load capacitance variation, we varied C_L from -30% to $+30\%$ of the nominal value while keeping all other components the same. The power was then measured. The results for a 1-MHz clock and a 100-pF load capacitance are plotted in Fig. 19. Normalized power dissipation in the graph is the ratio between the measured power dissipation and fC_LV^2. Power dissipation at 100 pF is minimum because the circuit is designed to harmonically resonate at this value. No frequency variation was noticed for this range of capacitances as is expected for any externally-driven driver. Unlike the self-oscillating rail drivers whose frequency varies proportional to the square root of variations in capacitance [5], this beneficial characteristic of our drivers significantly increases system stability. For capacitance greater than 130%, however, significant voltage-level degradation is observed. On the other hand, if we reduce the load capacitance below 70% of nominal, the power dissipation increases rapidly because current from the input pulse generator mostly charges the load capacitance instead of it being charged resonantly. In addition to the increased power dissipation by the load ca-

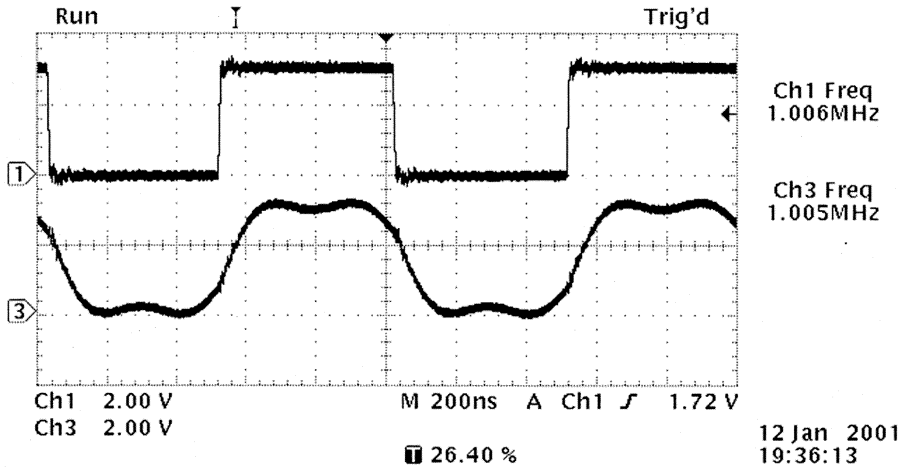


Fig. 15. Scope trace of output waveform for the second-order driver at 1 MHz.

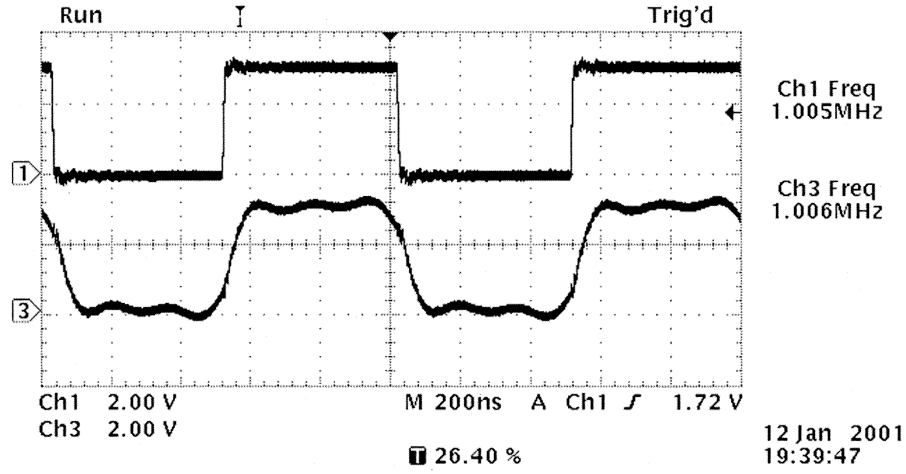


Fig. 16. Scope trace of output waveform for the third-order driver at 1 MHz.

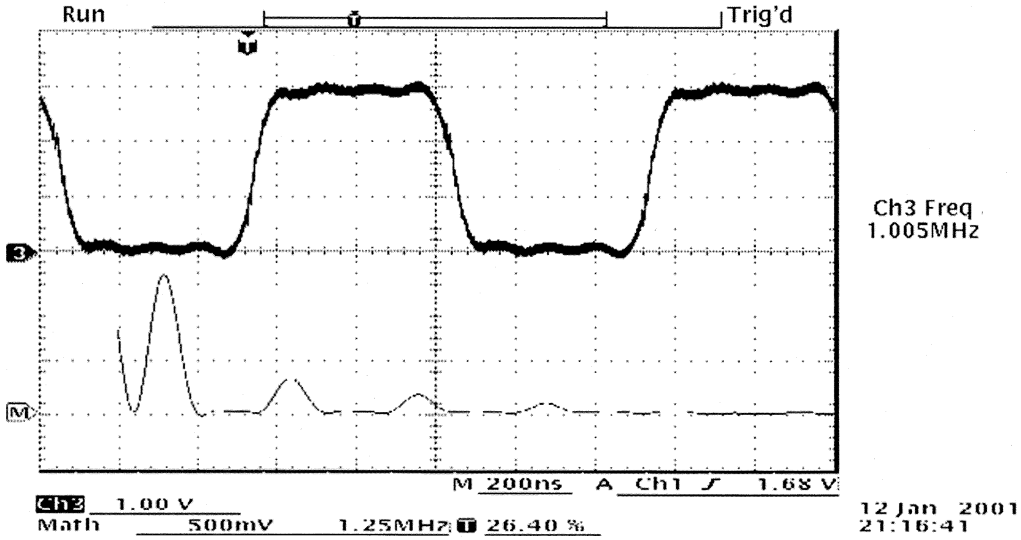


Fig. 17. FFT-enabled scope trace of waveform for the fourth-order driver at 1 MHz.

pacitance variation, the phase shift between the input pulse and the generated output causes clock jitter. To quantify this effect, we measured the delay time of the output with respect to the input pulse at the $Vdd/2$ voltage level while varying the load capacitance C_L from -30% to $+30\%$ of the nominal value. The measurement results are shown in Fig. 20. We observed clock jitter ranging from -47 to 43 ns for 1-MHz clock frequency. This relatively high clock jitter can be com-

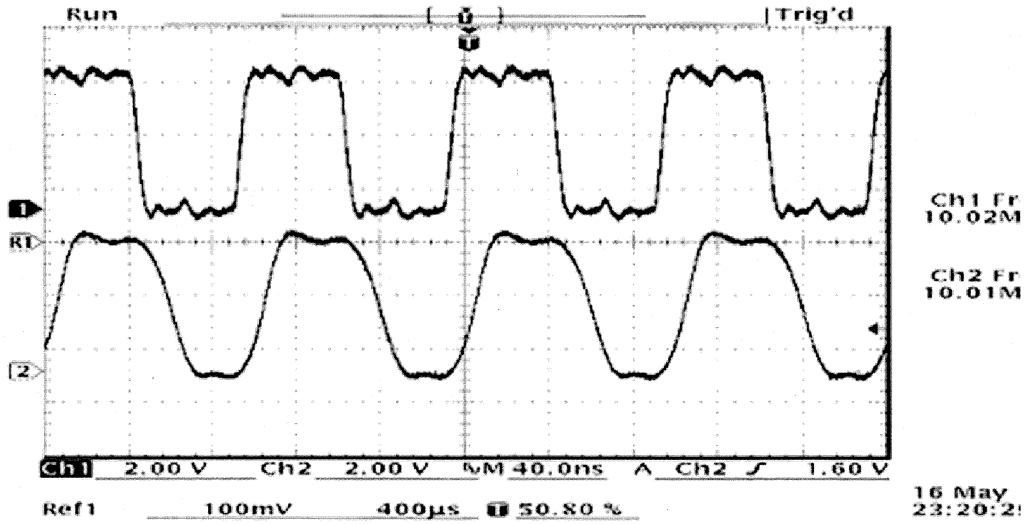


Fig. 18. Scope trace of output waveform for the second-order driver at 10 MHz.

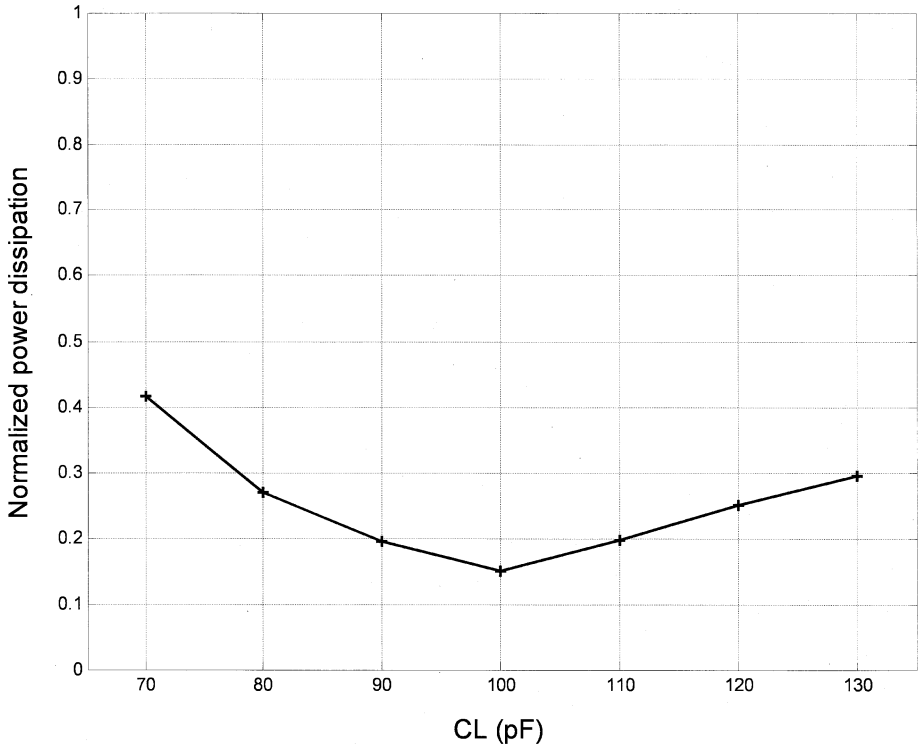


Fig. 19. Normalized power dissipation versus load capacitance (C_L). All components except C_L are kept same as designed for 100 pF C_L.

pensated by an increased clock cycle time. Therefore, 5% to 10% performance loss is expected for applications with high load capacitance variation.

Another experiment was carried out to measure power dissipation as a function of frequency change of the input pulse generator. We varied the frequency of the input pulse generator (f_{clk}) from -10% to $+10\%$ from its nominal value then the power was measured. Fig. 21 shows the measurement results of the power dissipation. At the nominal frequency (1 MHz), the normalized power dissipation is 14% of fC_LV^2. When f_{clk} is reduced by 10% from its nominal value, the power dissipation is increased to 39% of fC_LV^2. 36% of fC_LV^2 was measured when f_{clk} is increased by 10%. For 2% frequency fluctuation, the power dissipation is increased to 15% of fC_LV^2.

VI. Conclusion

In this paper, we presented a new algorithm and a prototype implementation of a harmonic resonant rail driver. The design goal was to produce an energy-efficient harmonic resonant clock signal using a simple network topology requiring no additional dc power supply. The experiment result shows that a significant amount of energy for driving the clock load can be recycled and saved by the resonant characteristic of the proposed driver.

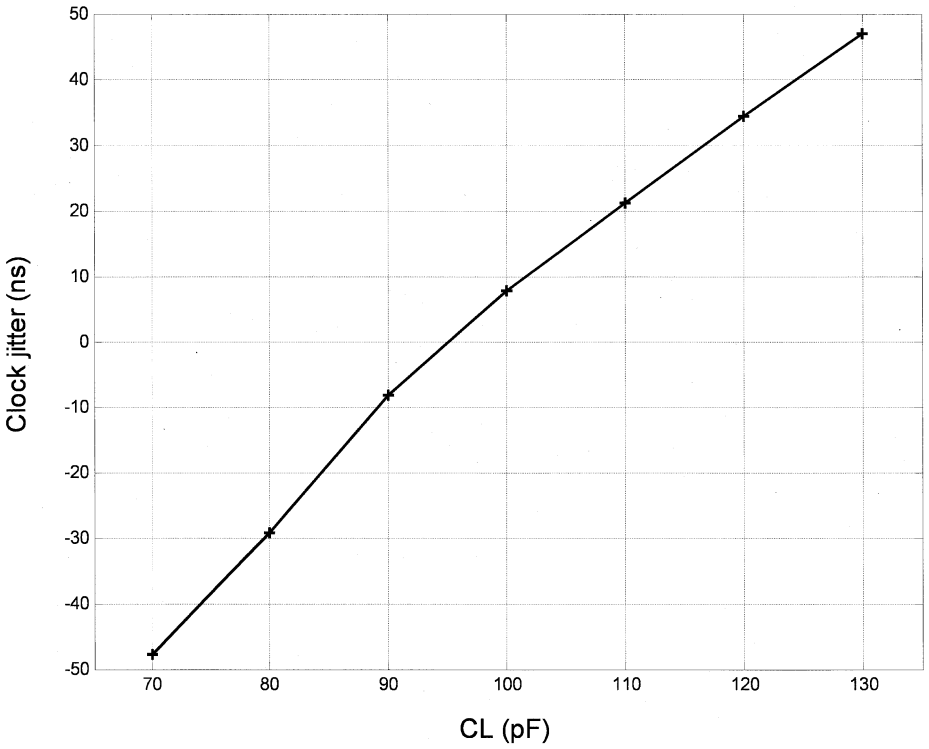


Fig. 20. Clock jitter versus load capacitance (C_L).

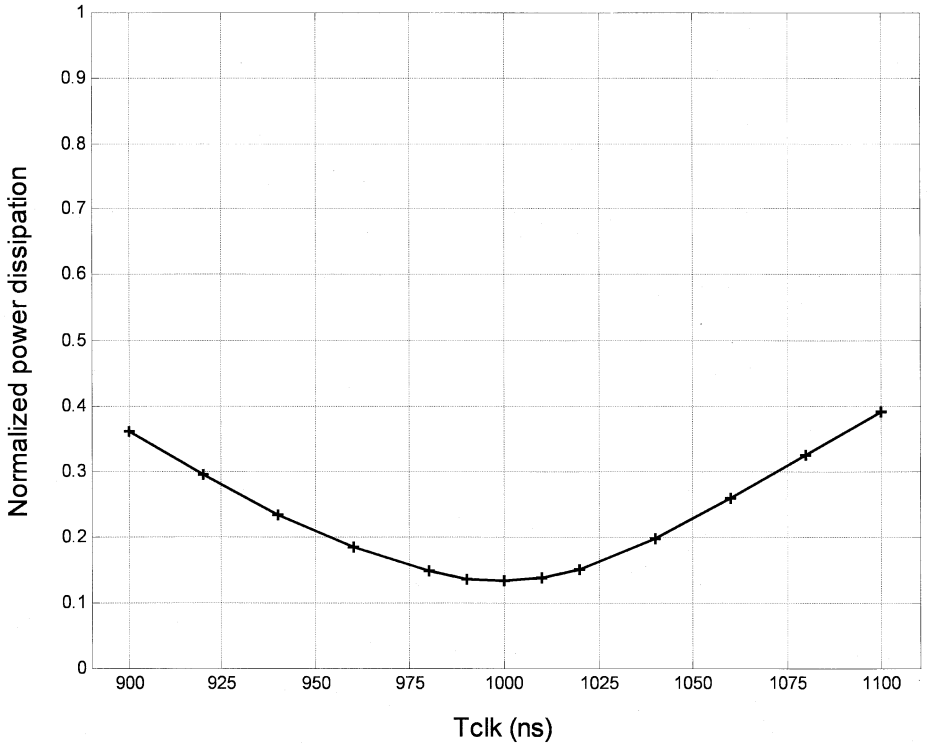


Fig. 21. Normalized power dissipation versus clock cycle variation.

Depending on the number of harmonics in the driver, we were able to save 70% to 85% of the conventional power dissipation. Moreover, our driver is much more robust than previously reported resonant clock drivers, in that it greatly reduces the frequency variation caused by changes in load capacitance.

Implementation with integrated inductor and capacitor requires further work. The straightforward procedure for implementing the external clock driver is to measure the load capacitance by driving it with a conventional clock driver and tune other components correspondingly. Therefore, high-accuracy capacitance extraction is crucial to integrate the driver inside ICs. A phase comparator and varactors to compensate error caused by capacitance estimation and load capacitance variation could be a feasible solution, but power dissipation will be

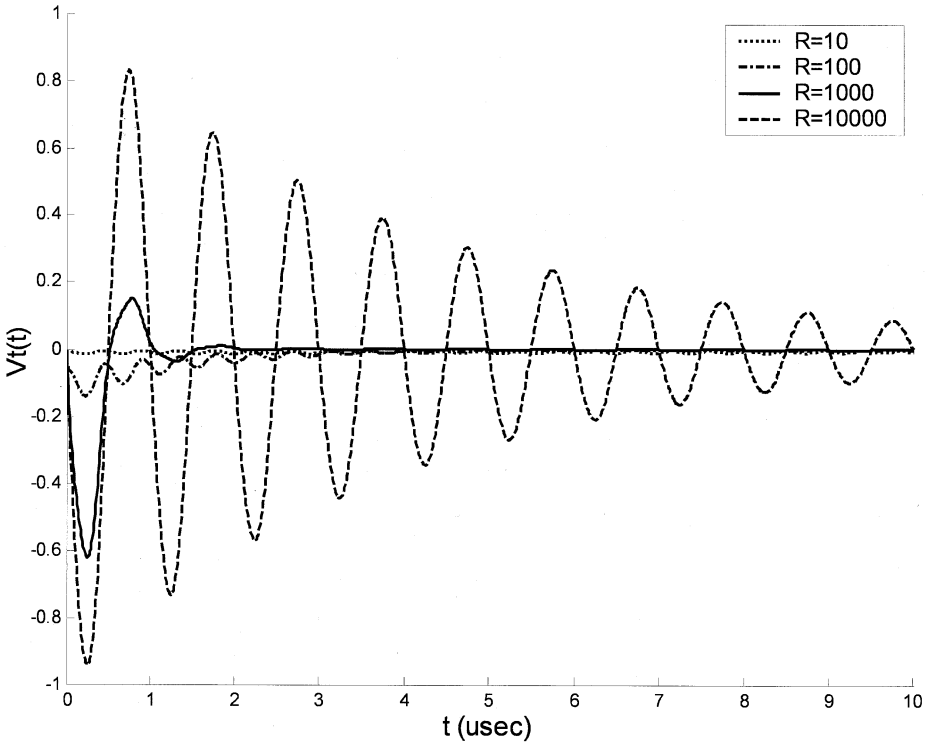


Fig. 22. Waveform plot for $v_x(t)$ in (46).

increased by these additional circuitries. In addition, the low-Q characteristic of the internal inductor may cause low power efficiency of the harmonic clock driver.

For high-frequency applications, the parasitic components of each inductor and capacitor will significantly affect the output waveform and power dissipation. Therefore, a simulation-based optimization strategy is needed to achieve optimum performance and power dissipation. Nevertheless, the theoretically-optimal circuit derived from our analysis can be the initial circuit for a more detailed nonlinear simulation-based optimization strategy. Providing such a good initial condition can dramatically reduce the run time of the simulation-based approach. In addition, the theoretic analysis may also be useful in guiding the search strategy.

APPENDIX
PROOF OF (33) FOR THE SECOND-ORDER DRIVER

By applying KCL on the output node of Fig. 8 (for the second-order driver), we can write the following:

$$\frac{V_i(s)-V_o(s)}{R}=\left(sC_L+\frac{1}{sL_0}+\frac{sC_1}{s^2L_1C_1+1}\right)\cdot V_o(s). \tag{38}$$

V_o can be rewritten as shown in (39) at the bottom of the page. For the second-order square-wave driver, all of the components can be represented with C_L and ω_0 as follows:

$$L_0=\frac{5}{9}\frac{1}{C_L\omega_0^2},\qquad L_1=\frac{5}{16}\frac{1}{C_L\omega_0^2},\qquad C_1=\frac{16}{25}C_L$$

$$\frac{1}{L_1C_1}=5\omega_0^2,\qquad \frac{1}{L_0C_L}=\frac{9}{5}\omega_0^2,\qquad \frac{1}{L_1C_L}=\frac{16}{5}\omega_0^2$$

$$\therefore\left(\frac{1}{L_1C_1}+\frac{1}{L_0C_L}+\frac{1}{L_1C_L}\right)=10\omega_0^2$$

$$\frac{1}{L_0L_1C_LC_1}=9\omega_0^4. \tag{40}$$

Using (40), we can simplify (39) into (41)

$$V_o(s)=\frac{1}{RC_L}\cdot\frac{s^3+5\omega_0^2s}{s^4+\frac{s^3}{RC_L}+10\omega_0^2s^2+\frac{5\omega_0^2s}{RC_L}+9\omega_0^4}\cdot V_i(s). \tag{41}$$

To show how input harmonic signals are not affected by the series resistor R, let us examine the output when sine wave $(V_i(t)=A_k\cdot\sin(k\omega_0t))$ is applied. Note that ideal square-wave is the sum of the sine waves harmonically related

$$\begin{aligned}V_o(s)&=\frac{(L_0L_1C_1s^3+L_0s)\cdot V_i(s)}{RL_0L_1C_LC_1s^4+L_0L_1C_1s^3+R(L_0C_L+L_1C_1+L_0C_1)s^2+L_0s+R}\\&=\frac{\left(s^3+\frac{s}{L_1C_1}\right)\cdot\frac{V_i(s)}{RC_L}}{s^4+\frac{s^3}{RC_L}+\left(\frac{1}{L_1C_1}+\frac{1}{L_0C_L}+\frac{1}{L_1C_L}\right)s^2+\frac{s}{RL_1C_LC_1}+\frac{1}{L_0L_1C_LC_1}}\end{aligned} \tag{39}$$

($k = 1, 3, \ldots$). Using partial fraction expansion, the following can be established

$$V_o(s) = \frac{A_k}{RC_L} \times \left(\frac{\alpha s^3 + \beta s^2 + \gamma s + \lambda}{s^4 + \frac{s^3}{RC_L} + 10\omega_0^2 s^2 + \frac{5\omega_0^2 s}{RC_L} + 9\omega_0^4} + \frac{\theta s + \sigma}{s^2 + k^2\omega_0^2} \right). \quad (42)$$

By comparing (41) and (42), we find

$$\begin{aligned} &(\alpha+\theta)s^5 + \left(\sigma + \beta + \frac{\theta}{RC_L}\right)s^4 \\ &\quad + \left(\alpha k^2\omega_0^2 + \gamma + \frac{\sigma}{RC_L} + 10\theta\omega_0^2\right)s^3 \\ &\quad + \left(\beta k^2\omega_0^2 + \lambda + 10\sigma\omega_0^2 + \frac{5\theta\omega_0^2}{RC_L}\right)s^2 \\ &\quad + \left(\gamma k^2\omega_0^2 + \frac{5\sigma\omega_0^2}{RC_L} + 9\theta\omega_0^4\right)s + (\lambda k^2\omega_0^2 + 9\sigma\omega_0^4) \\ &\quad = k\omega_0 s^3 + 5k\omega_0^3 s. \end{aligned} \quad (43)$$

Solving for θ and σ

$$\frac{(1-k^2)(9-k^2)}{k^2}\sigma + \frac{1}{RC_L}(5-k^2)\omega_0^2\theta = 0. \quad (44)$$

Notice that when $k = 1$ and 3, θ is forced to zero which in turn simplifies other terms as shown below

$$\begin{aligned} \alpha &= 0 \\ \beta &= -RC_L k\omega_0 \\ \gamma &= 0 \\ \lambda &= -\frac{9RC_L}{k}\omega_0^2 \\ \sigma &= RC_L k\omega_0 \\ \theta &= 0. \end{aligned} \quad (45)$$

Therefore, for $k = 1$ or 3, (42) becomes

$$\begin{aligned} V_o(s) &= V_x(s) + V_i(s) \\ &= \frac{A_k}{RC_L} \\ &\quad \times \left(\frac{-RC_L k\omega_0 s^2 - \frac{9RC_L\omega_0^2}{k}}{s^4 + \frac{s^3}{RC_L} + 10\omega_0^2 s^2 + \frac{5\omega_0^2 s}{RC_L} + 9\omega_0^4} + \frac{RC_L k\omega_0}{s^2 + k^2\omega_0^2} \right) \\ &= \frac{-A_k k\omega_0 s^2 - \frac{9A_k\omega_0^2}{k}}{s^4 + \frac{s^3}{RC_L} + 10\omega_0^2 s^2 + \frac{5\omega_0^2 s}{RC_L} + 9\omega_0^4} + \frac{A_k k\omega_0}{s^2 + k^2\omega_0^2}. \end{aligned} \quad (46)$$

From this equation, we can conclude the first two harmonics from the input pulse generator are not affected by the series resistor and thus appear at the output node with the same magnitude and phase. Fig. 22 shows the time-domain waveform of $V_x(s)$ for various R values. As shown in the figure, the magnitude of $v_x(t)$ always converges to zero regardless of R value. Therefore, when the circuit reaches steady-state condition, only the first two harmonics are present at the output node and no power is dissipated if the input is composed of these two harmonics.

REFERENCES

[1] J. Rabaey, *Digital Integrated Circuits: A Design Perspective*. Englewood Cliffs, NJ: Prentice-Hall, 1995.

[2] W. Athas, N. Tzartzanis, L. Svensson, and L. Peterson, "A low-power microprocessor based on resonant energy," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1693–1701, Nov. 1997.

[3] W. Athas, L. Svensson, and N. Tzartzanis, "A resonant signal driver for two-phase, almost-nonoverlapping clocks," in *Proc. Int. Symp. Circuits and Systems*, 1996, pp. 129–132.

[4] W. Athas, N. Tzartzanis, W. Mao, L. Peterson, R. Lal, K. Chong, J.-S. Moon, L. Svensson, and M. Bolotski, "The design and implementation of a low-power clock-powered microprocessor," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1561–1570, Nov. 2000.

[5] N. Tzartzanis, "Energy-recovery technique for CMOS microprocessor design," Ph.D. dissertation, Dept. Elect. Eng., Univ. of Southern California, Los Angeles, CA, 1998.

[6] W. Athas, L. Svensson, J. Koller, N. Tzartzanis, and Y. Chou, "Low-power digital systems based on adiabatic-switching principles," *IEEE Trans. VLSI Syst.*, vol. 2, pp. 398–406, Dec. 1994.

[7] J. Denker, "A review of adiabatic computing," in *Proc. 1994 Symp. Low-Power Electronics*, 1994, pp. 94–97.

[8] S. Younis and T. Knight, "Non-dissipative rail drivers for adiabatic circuits," in *Proc. 16th Conf. Advanced Research VLSI*, 1995, pp. 404–414.

[9] G. Glasoe and J. Lebacqz, Eds., *Pulse Generator*. New York: McGraw-Hill, 1948, pp. 175–224.

[10] M. Van Valkenburg, *Network Analysis*. Englewood Cliffs, NJ: Prentice-Hall, 1974.

[11] *Coilcraft Document 112-1, Slot Seven 7mm Tunable Inductor Data Sheet*. Cary, IL: Coilcraft, Inc., 2001.

Joong-Seok Moon (S'97–M'03) received the B.S.E.E. and M.S.E.E. degrees from the Seoul National University, Korea, in 1993 and 1995, respectively, and the Ph.D. degree in electrical engineering from the University of Southern California, Los Angeles, in 2003.

Currently, he is a VLSI Application Engineering with Apple Computer, Inc, Cupertino, CA. From 1995 to 1996, he was a VLSI Engineer with Samsung Electronics, Korea. He was also with Information Sciences Institutes, University of Southern California, Marina del Rey, CA where he was involved in several VLSI research projects such as low–power microprocessor, feedback cancellation DSP chip for hearing-aid, low-power FIFO SRAM, and floating–point unit for DIVA processor-in-memory processor. His research interests include are low-power circuit and system design for general purpose and DSP architecture.

William C. Athas (M'99) received the B.S. degree in computer science from the University of Utah, Salt Lake City, in 1978, and the Ph.D. degree from the California Institute of Technology, Pasadena, CA, in 1987.

In 2000, he joined Apple Computer, Inc., Cupertino, CA, where he is a VLSI Systems Architect and Principal Engineer in the VLSI-Hardware Engineering Department. At Apple he works in the areas of high-speeding signaling, mixed-signal integrated-circuit designs, microprocessor speed and power modeling, and advanced microarchitecture concepts and designs. From 1991 to 2000, he was a Research Scientist and Senior Project Leader with the Information Sciences Institute, University of Southern California, Marina del Rey, CA. During this time he was the Team Leader for the design and implementation of the AC1 microprocessor, which demonstrated a new approach to low-power computing based on the principle of energy recovery. He has 23 publications in the areas of the theory and design of low-power circuits and high-performance computer architecture. He has received patents for low-power and asynchronous circuits, high-performance memory subsystems, and network hardware.

Sigfrid D. Soli photograph and biography not available at the time of publication.

Jeffrey T. Draper (S'85–M'89) received the B.S. degree in electrical engineering from Texas A&M University, College Station, TX, in 1987, and the M.S.E. and Ph.D. degrees in electrical engineering from University of Texas, Austin, TX, in 1990 and 1993, respectively.

He is a Research Assistant Professor at the University of Southern California (USC), Los Angeles, and is also a Project Leader with the Information Sciences Institute, USC, where he has been working in research since 1993. He has led the VLSI effort on several DARPA-funded projects and has produced a number of complex ICs, with the most recent chip fabricated in 0.18 μm technology and containing 55 million transistors.

Peter A. Beerel (S'88–M'95) received the B.S.E. degree in electrical engineering from Princeton University, Princeton, NJ, in 1989, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1991 and 1994, respectively.

Currently, he is the Vice-President of Asynchronous Computer-Aided Design and Verification at Fulcrum Microsystems, Inc., Calabasas Hills, CA, a startup company developing and commercializing asynchronous designs. He is also an Associate Professor, currently on leave, from the Department of Electrical Engineering-Systems at the University of Southern California (USC), Los Angeles. He has consulted for Yuni Networks and AMCC in the areas of networking chip design, Intel, and asynchronous digital design in the areas of asynchronous design and computer-aided design, and TrellisWare Technologies in the area of communication chip design. His research interests include a variety of topics in CAD and VLSI.

Dr. Beerel received the Outstanding Teaching Award in 1997 and the Junior Research Award in 1998, from the School of Engineering, USC. He received a National Science Foundation (NSF) Career Award and a 1995 Zumberge Fellowship. He was also co-recipient of the Charles E. Molnar Award for two papers published in ASYNC'97 that best bridged theory and practice of asynchronous system design and was a co-recipient of the best paper award in ASYNC'99. He is coauthor of four patents in the area of asynchronous circuits. He has been a Member of the Technical Program Committee for the International Symposium on Advanced Research in Asynchronous Circuits and Systems since 1997 and was Program Co-chair for ASYNC'98. He has served on the Technical Program Committee for the International Conference on Computer-Aided Design in 2000 and 2001.